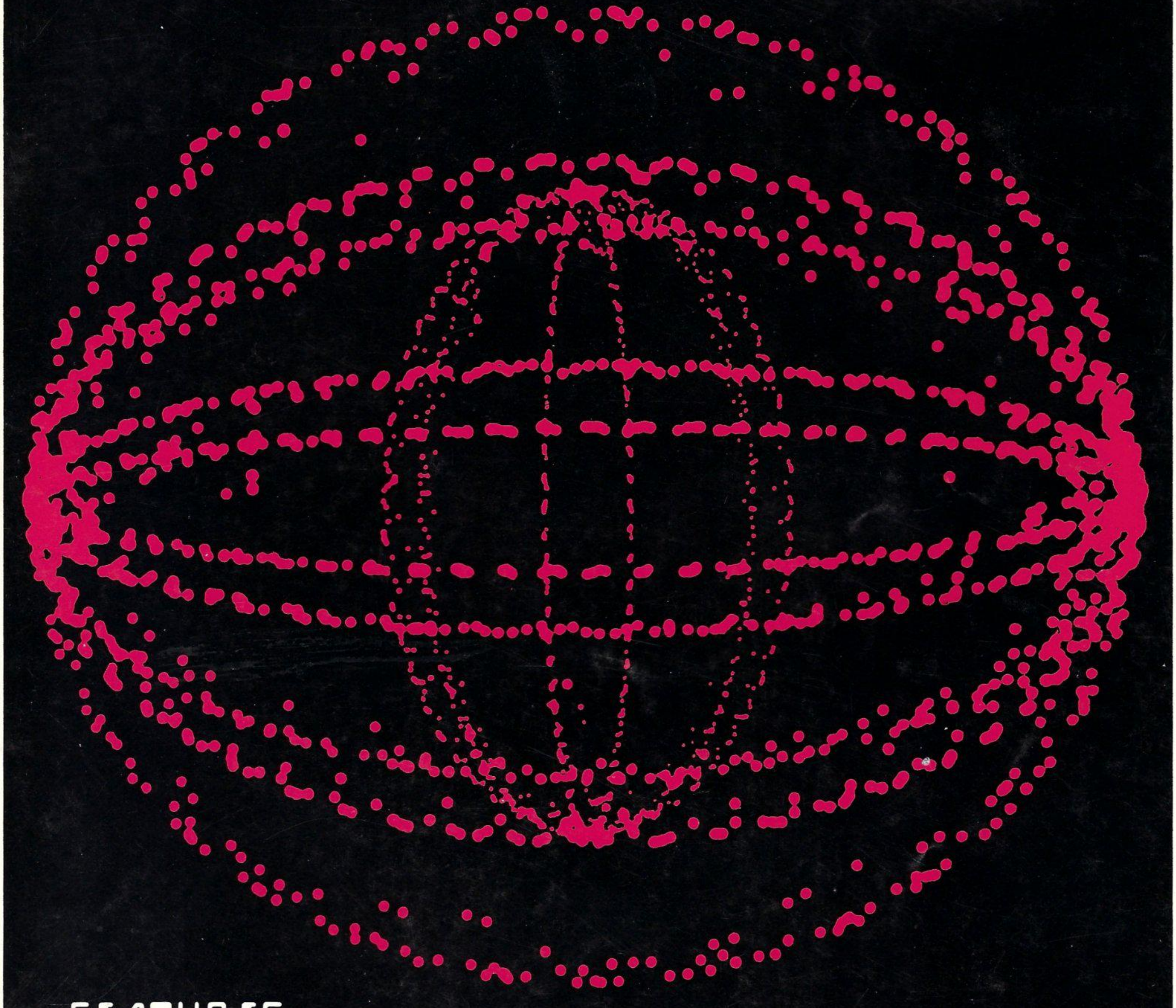
VOL. 1 ISSUE 3 FEBRUARY 1976

SCCS INTERFACE

THE NATIONAL PUBLICATION OF THE SOUTHERN CALIFORNIA COMPUTER SOCIETY



FEATURES

Introduction to Microprocessor Technology

Timing by Use of Microcomputers

Further Reflections of a Culture Savage

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THE SOUTHERN CALIFORNIA COMPUTER SOCIETY

OBJECTIVES

A non-profit organization whose purpose is:

A. To exchange and disseminate information among the Society members concerning the computer arts and sciences.

B. To provide a technical assistance to other members of the Society in those computer projects which are not undertaken for pecuniary gain or profit including but not limited to hardware, software, and computer programming.

C. To publish books, newsletters, magazines, and other periodicals for the benefit and education of the Society members and the general public.

D. To conduct and sponsor seminars, lectures, and courses relating to the computer arts and sciences.

F. To develop and maintain computer centers and laboratory workshops for the members of the Society and the general public including provisions for time-sharing operations.

PUBLICATIONS

SCC INTERFACE, the official publication of the Southern California Computer Society is published monthly. Its content is composed primarily of articles contributed by members of the Society and intended for the reader with an interest in computers for professional or avocational reasons.

MEMBERSHIP

Membership in the Society is open to anyone, regardless of educational background or geographic location. All members are entitled to the rights of meetings, elections, receipt of official publications in a timely manner, and all other benefits as provided by the officers, Board of Directors, and various committees of the Society pursuant to the by-laws of the Southern California Computer Society.

MEMBERSHIP CLASSIFIED ADVERTISING

Each month SCCS Interface will devote some space free, non-commercial advertising by members. This is done as a service to members of the Southern California Computer Society and to help promote communications between computer experimenters and hobbyists throughout the world.

Many SCCS members, being pioneers in the small computer field, often have for sale, on an occasional basis, used computing equipment, or equipment they have designed and built themselves. Those members, as well as those who simply wish to establish contact with individuals with similar or complimentary interests, are encouraged to utilize the member ad privilege subject to the following conditions:

A. Ads must be received by the ad editor of SCCS Interface by the first of the month prior to issue month.
B. Ads may list the member's name, home address and phone. No commercial firm names, please!
C. Ads must be typewritten, double spaced and no more than 250 characters (including spaces and punctuation) in length. Ads 250-500 characters will be printed on space-available basis.
D. Ads may be run up to three consecutive issues, however, a specific request must be received for each instance.
E. No free member ads will be accepted for the sale of equipment or services by a commercial profit-oriented individual or organization.

Address all member ads to:

Interface Ad Editor, Nancy DeLong, 8005 Denrock Ave., Los Angeles, Calif. 90045

Those non-members wishing to advertise are invited to join SCCS and enjoy the member ad privilege as well as the delivery of SCCS INTERFACE to your mail box.

PUBLISHER

McPHETERS, WOLFE & JONES, 6515 Sunset Blvd., Suite 202, Hollywood, California 90028

All editorial content and effort are contributed at no cost to the Society. Opinions expressed in by-lined articles do not necessarily reflect the opinion of this magazine or the Southern California Computer Society. Mention of products by trade name in editorial material or advertisements contained herein in no way constitutes an endorsement of the product or products by this magazine or by the Southern California Computer Society.

DISPLAY ADVERTISING

Direct all advertising inquiries to:

Advertising Department
SCCS INTERFACE - ADVERTISING DEPARTMENT
61 S. Lake Ave.
P.O. Box 4566
Pasadena, Calif. 91106
(213) 681-0685

CONTRIBUTIONS

They must be accompanied by return postage and we assume no responsibility for loss or damage thereto. Any material accepted is subject to such revision as is necessary in our sole discretion to meet the requirements of this publication. The act of mailing a manuscript and/or material shall constitute an express warranty by the contributor that the material is original and in no way an infringement upon the rights of others. Send all contributions to: Art Childs - Editor, 335 North Adams, Suite 210, Glendale, Ca. 91206

sccs INTERFACE
The National Publication of the Southern California Computer Society
Vol. 1 Issue 3 Feburary 1976

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COVER STORY

John Whitney, whose career in art/technology began in 1940, pioneered projects in computer graphics art in 1965 under an IBM research grant. In the fall of 1975 he completed a film entitled "ARABESQUE", supported by a grant from the National Endowment for the Arts. Mr. Whitney is continuing proseminars in design with the electronic image at UCLA.

Colonel Beauregard Heiser: founder of the oldest and most complete computer store.

ALTAIR 8800 COMPUTER
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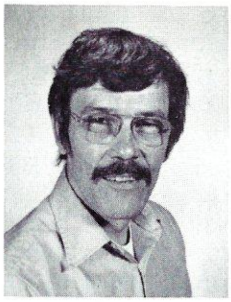


Art Childs, Editor

Photo by George R. Clarke

INTERFACIAL

Our order of priorities for basic need fulfillment are food, shelter, protection and pleasure. With hunger satisfied, man builds his house. With the house completed he fights to protect it. Only with these first objectives satisfied does man turn to pleasure gratification, whether it's sexual, frivolous, or aesthetic in nature. Perhaps the time for aesthetic pleasure has arrived for the computer buff.

For thousands of years man has set upon rock, parchment and canvas perceptions of his experience and environment. Initially attempts at art captured only single moments, or depicted but a miniscule feeling, and necessarily so. His tools were limited.

From colored mud and a stick, to parchment, ink and a quill pen, man progressed in the expression of his ideas and feelings from oil and canvas to plentiful paper and high speed printing processes. He has at last achieved dissemination to the masses, the results of his expressive efforts. Even now increasingly more aspects of our lives are touched by these efforts with blue prints and wiring diagrams, lithographically reproduced masterpieces and comic strips, paperback novels and dictionaries — the list is almost endless.

With the possible exception of stage plays, it was not until the invention of the movie camera that the dimension of dynamics was added to the visual arts, nor was it until the invention of the oscilloscope that the dimension of dynamics was added to technical graphics. And now, almost suddenly, dynamic graphics aided by economical computing power, is upon us.

We've all seen or heard of many applications of dynamic graphics in science and industry — a drawing of a proposed building on a CRT being slowly rotated so that it may be perceived from all sides, or a graphic representation of the runway and horizon on the CRT of an aircraft flight simulator. Dynamics is piercing the world of visual art. Witness the span from simple multi-colored and strobe lights responding to audio input, to the lasarium light show. Frank Zappa, coordinating rock music, video tape and computers, has created electrically a dynamic video and audio experience, leading the evolution to another new art form.

In a recent phone conversation with Carl Helmers of BYTE Magazine, I discovered he uses as an analogy when discussing the future of home computing, the history of the automobile. Helmers likens the current state of home computing to pre-World War II automotive days. If his view — one which I share — is realistic, we can look forward to exciting times filled with fascinating developments.

It is doubtful that Henry Ford envisioned, even in vague terms, the full impact of his contribution to transportation as he started production of the Model T. It is equally doubtful that Intel's crystal ball portrays the future with any greater clarity, but we live in an age that has taught us to expect technological miracles of both major and minor proportions.

I'm reminded of the supposedly true story about the senator who in the late 1800's introduced a bill to close the U.S. Patent Office for, as he is supposed to have declared, "All that can possible be invented has been invented!" A few short months later, a couple of bicycle mechanics flew one of the first airplanes.

At the other extreme, I think of the Buck Rogers comics of the 1930's and 40's, and then the television series "Startrek", with faster - than - the - speed - of - light space travel and that great transportation mechanism, "teleportation", where person and possessions are "beamed" from point to point instantaneously. (What would that do for the energy crises?)

Reality is apparently someplace between the two extremes. Still, with each new announcement of scientific and technological achievement, it seems that for the computer buff the latter extreme will soon be fact.

Thus far in the field of computer technology the emphasis has been placed on the solution of practical problems. Just as the automobile had to be developed to a state of economic reliability before it could become an instrument of sport and pleasure, the computer had to be developed to a similar state before it could be used as a tool for pleasure and art.

Now that the necessary development has occurred, the first of the pleasure tasks for computers has arrived — GAMES. Hunt The Wampus, Life, Startrek, and many others exist with more being written daily. Another pleasure task for computers, one of a more aesthetic nature, is coming over the horizon — real-time computer art — dynamic graphics using as an output device an instrument that already resides in most American homes — the color TV set.

And what of the computer hobbyist in all this? John Whitney in the featurette on page presents a challenge to the artistically inclined computer buff. Using a computer, a CRT (color TV set), the necessary interfacing hardware and a lot of imagination, a new art, still in its formative stages, will begin the journey that hopefully will culminate in the emergence of the Brahms, Beethovens and Bachs of the visual dynamic arts.

Many possibilities for exploration come to mind. Colorful, aesthetically pleasing geometric patterns that change in size, shape, color and intensity in response to musical input, could add a dimension of Tchaikovsky's genius heretofore unexperienced. The completely creative task of dynamically expressing simple moods and feelings with bright colors and flowing lines could well become a modern version of finger painting. Even therapeutic possibilities exist; it seems infinitely preferable to relax in front of a TV screen filled with flowing lines, changing colors and emerging shapes rather than portrayals of inhumane violence and other "boob tube" garbage currently on display.

Just as advancements in metallurgy and energy conversion gave us automative transportation, the advent of semiconductors is giving us the possiblity of new artistic experience. The technical tools are within reach. The only limitation we need labor under is the inhibition of our imagination.

IN THIS ISSUE . . .

In addition to the continuation of the THEORY OF MICROPROCESSOR TECHNOLOGY, and Cliff Sparks' Teleprinter Maintenance and Repair series, our hard working hardware editor, Scott Wilcox takes a look at a 4K Altair compatible memory kit. Scott also examines closely power supplies and associated problems for those of us who intend to load our machines with extensive hardware interfaces and memory. He then presents a circuit of interest to purchasers of the Processor Technology 3P+S. Finally, Scott reports on further developments in the Godbout 4K memory board.

Terry Benson, an applications engineer with Intel, leads off the software side of the fence with the first of a series of articles dealing with the use of the 8080 as a timing device. Terry's contribution will be of special interest to the novice programmer as he discusses many of the basics involved in applications development.

Don Tarbell provides further assistance to the beginner in the form of a disassembler written in basic.

A new member and programmer with Telaid, Lorne Douglas has contributed a trace routine. The "Bug Chaser" is a valuable education tool as well as a handy device for ferreting out those program gremlins that all too frequently haunt the assembly language programmer.

Besides the usual club news, the **Update** section contains two items of special interest. One has to do with the Altair Convention coming up in late March. MITS appears to be going all out to provide an interesting and informative weekend in Albuquerque. The second item announces the formation of the San Fernando Valley Chapter of SCCS. In addition to providing the advantages of a smaller group within SCCS, it is hoped the SFV chapter will give us the necessary experience to promote smooth and effective chapter formation in other areas.

That Thin Line
or
Between a Rock and a Hard Spot

Enter Irate Club Member, stage left.
Enter Irate Manufacturer, stage right.
Enter Irate Publisher, center.
Enter Editor, fearfully.

Club Member: "Wha's a big idea selling out to you-know-who. This is supposed to be a club magazine not another commercial put-on. Boy, you can't tell me you're not in bed with 'em—you've even put their picture on the cover."

Manufacturer: "Sir, in our opinion, your editorial policies are not conducive to mutually beneficial cooperation between our respective organizations. We feel you unfairly print comments and articles which cast unwarranted aspersions on our impeccable image."

Publisher: "Look, Art, this is the real world we live in. Like it or not, you've got to please all the people, all the time."

Club Member, exiting stage left: "Traitor!"
Manufacturer, exiting stage right: "Socialist!"
Publisher, just exiting: "For shame, for shame!"

Stage lights dim slowly.

Editor, bewildered, muttering: "Uh—let's see now—all the time, all the people. No—time the people—no—uh—Please the time—uh—let's see—

```
LDA PEOPLE
LXI H, TIME
MOV M,A
INX H
CPI PLEASE
JM OBLIVION
```

Yean, now I got it!"

Stage lights out. Curtain down.

END ACT I

First Annual

WACC!

World Altair Computer Convention

This year's most exciting computer convention could very well be the First Annual WORLD ALTAIR COMPUTER CONVENTION. Computer hobbyists from all over the World will gather in Albuquerque, New Mexico on Saturday and Sunday, March 27 & 28. Many of them will be bringing their Altair systems in order to compete for the $10,000 worth of Altair equipment to be given away at the convention. In addition to demonstrations of Altair product applications, there will be FOUR SEMINARS presented during this dynamic weekend.

SEMINAR ONE will be a seminar on LOW COST COMPUTING conducted by some of the leading figures in the field. A preliminary list of speakers includes Larry Steckler, technical editor of Radio Electronics, Carl Helmers, editor of Byte magazine, Art Childs, editor of Interface magazine, David Ahl, publisher of Creative Computing, Judge Pierce Young, president and founder of the Southern California Computer Society, and Terry Silver, also of the SCCS. And this is only the beginning.

SEMINAR TWO will be a complete discussion of ALTAIR PRODUCTS and Altair design philosophy. Speakers will include H. Edward Roberts, president of MITS, Inc.; Project Engineers Bill Yates, Bob Zaller, Tom Durston, and Pat Goding; Software Writers Paul Allen and Bill Gates; and Computer Notes editor, David Bunnell.

SEMINAR THREE will be a presentation of the updated MITS TRAVELING SEMINAR presented by Pat Ward. Altair technical binders will be given away free to people attending this seminar.

SEMINAR FOUR will be an organizational meeting of the Altair Users Group conducted by Barbara Sims and David Bunnell. Topics will include organization of the Users Group and ways to improve MITS service to Altair users. All seminars will be opened to the audience for questions.

Attendance to the WORLD ALTAIR COMPUTER CONVENTION will be **free to all Altair owners and out of town guests.** The convention will be held at the new MITS building at 2450 Alamo SE, within walking distance of the Albuquerque Airport Terminal. The entire Airport Marina Hotel has been reserved for this occasion. Reservations at this hotel (which is also within walking distance of MITS and the Airport Terminal) can be made by filling out the coupon in this ad and returning it prior to February 26. Cost of reservations are $20 per night for a single and $24 for a double.

$10,000

MITS will be presenting door prizes and prizes for the best demonstrations at the convention. These prizes will include Altair 8800's, Altair 680's, and related equipment of a retail value not less than $10,000. To enter in this contest or to have a booth at the convention, you must fill out an official application form from MITS, Inc. Rules and regulations governing demonstrations and booths are available with application forms.

ALTAIR CONVENTION COUPON

Name____________________

Address____________________

City____________ State & Zip____________

☐ Yes, I plan to attend the first annual WACC to be held in Albuquerque, New Mexico on March 27 and 28, 1976.

☐ Please reserve a room for me at the Albuquerque Marina Hotel. I will need a ☐ single ☐ double room. I plan on staying in Albuquerque the following nights: ☐ Friday ☐ Saturday ☐ Sunday.

☐ Please send me the official entry form for the Altair Demonstration Contest.

MITS/2450 Alamo SE/Albuquerque, 87106 505-262-1951

UPdate

FEBRUARY MEETING — Saturday, the 21st.
TRW Systems, Redondo Beach
Building "S" Cafeteria
Doors open 10:00 am. Coffee hour is 12:00-1:00 pm.
Meeting 1:00-4:30 pm.

WORLD ALTAIR COMPUTER CONVENTION

MITS, Inc. has announced sponsorship of their first annual WORLD ALTAIR COMPUTER CONVENTION (WACC) set for March 27th and 28th to be held at the Albuquerque Airport Marina Hotel. All home computerists, or interested seekers of computer truth, are invited to attend admission free.

WHAT TO EXPECT

Early Friday evening (March 26th) arrivals may enjoy a demonstration via the MITSmobile which has been upgraded and expanded to reveal the latest ALTAIR developments.

On Saturday and Sunday, presentations by MITS engineers and software writers will feature discussion and display of all available ALTAIR products, design and future projections. On a broader scope the convention will be directed to low cost hobby computing in all its aspects.

Among the speakers to be highlighted, is Carl Helmers, editor of BYTE Magazine, who will talk on Trends and Applications for the Hobbyist. David Ahl, editor of CREATIVE COMPUTING, and author of "1001 Basic Games" will speak on kit building in schools. Also addressing a seminar is Larry Steckler, Technical Editor of "Radio Electronics" Magazine.

PRIZES TO BE AWARDED

MITS is giving away $10,000 in Altair kits as awards and door prizes. Four awards for the best demonstrations in two categories will be given. Winners with complete systems will be selected for the most innovative overall Altair system, and/or for the most exciting, dynamic home brew option or interface. The judges are people who are recognized professionals in the computer community outside the MITS family. Entry must be requested in advance, so start thinking now about your contest entries, and get your requests in to David Bunnell by February 25th.

Demonstration booths for manufacturers and retailers of in-user developed hardware and software will be available. To obtain information for contest entry approval and booth space, write to David Bunnell, WACC/MITS, 2450 Alamo, S.E., Albuquerque, New Mexico 87106.

Says Bunnell, "This convention will be the low cost computer's answer to NCC. We hope to bring together all leaders in the home computing field. Our purpose is to inform Altair users, and all computer hobbyists, of our product and projections for the future. We expect an attendance of at least 1,000 and hope that it becomes an annual event that will be the most exciting computer convention in the industry".

SPECIAL TRAVEL ARRANGEMENTS FOR SCCS MEMBERS

Group reservations for 100 members have been made through Leda Alpert of Majestic Travel, Inc., in Beverly Hills, which include round trip air travel on Texas International Airlines from Los Angeles International Airport. Twenty-five reservations have been made for Friday, March 26th departing late afternoon and arriving in Albuquerque approximately 8 pm. Travelers will enjoy a steak and wine dinner en route. Exact times can be confirmed by Leda Alpert. Saturday, March 27th, 75 seats are being held and departure time is set for 8 am, arriving in Albuquerque at 10:36. Breakfast of reputedly excellent faire will be served on board. Air reservations are available on a first come, first serve basis, but additional space arrangements will be made if an overwhelming number of members turns out early enough. Airfare is $104.73 round trip.

FOR MEMBERS EAST OF CHICAGO

For those SCCS members who live east of Chicago, a travel group may be formed for equally beneficial travel discounts by contacting Barry Brooks at Raleigh Travel. The phone number is (212) 486-1172. If you have been considering becoming a member, now would be a good time to join. You'll more than save the annual membership dues in travel savings.

ALL THIS AND HOTEL TOO!

Accommodations at the Airport Marina Hotel in Albuquerque include complimentary coach service to and from the airport, and a hospitality suite for the Southern California Computer Society. Rates are $20 for single, and $24 for double. Additional information and itinerary can be obtained by calling Miss Alpert at (213) 657-0441 or (213) 451-5232. Reservations, accompanied by a $50 deposit, must be in no later than February 26th.

SPECIAL THANKS TO LEDA ALPERT

Those of us at INTERFACE, as well as the members of the Board of Directors and the Officers of SCCS are grateful for the volunteer work of Leda Alpert in coordinating Board and Committee meetings. Leda spends many hours on the telephone to assure that persons concerned are notified.

If members are planning personal or business travel, please call her for travel and accommodations reservations. The service she can provide will offer added convenience without additional cost. She has arranged several business trips for our members and provides personalized service at the lowest possible cost, as well as special group rates for SCCS members, who travel in groups of ten or more.

SOUTH EAST COMPUTER GROUP

South East Computer Group is holding meetings the first Thursday of every month, reports SCCS member D. Ekstrand. Meetings are being held at Southgate Public Library, 4035 Tweedy, Southgate, 90280 from 6:30 p.m. to 9:00 p.m. For information call (213) 566-1677.

EDUCATION UPDATE

SCCS has finally kicked off an EDUCATION PROGRAM that's quite exciting. For the "hardware types" we are now running APL and BASIC classes and for the "software types" we have a class on teletype maintenance and a CPU design/construction workshop underway. A construction techniques class and an introduction to digital devices and circuits are on the drawing board now.

At the last general meeting several other courses were suggested and requested. For example: a workshop to build an 8080 APL interpreter, ANYTHING for the rank engineer, how to use an oscilloscope, a workshop to construct ALTAIR accessory boards (memory, I/O, etc.), a trouble-shooting class, a workshop for the design and construction of a digital stopwatch (see RADIO ELECTRONICS, November 1975), a workshop to build diagnostic routines for the ALTAIR 8800 and 680, a workshop to construct equipment such as scopes, digital probes, multimeters, and breadboard testers, a workshop to design and build power supplies, etc.

If you would like to lead one of these, or some other sort of class or design/construction workshop, let's hear from you (use the form below). The policy for fees is not finalized, but the class tuition will probably be divided between the leader of the group, SCCS, and the cost of components (if any). SCCS will also subsidize classes if necessary.

Finally, to acknowledge the people who have been responsible for getting this phase of SCCS activity off the ground: Larry Press, Coordinator, Pat Amornvitikimcha, Marv Perlman, Jerry Silver, Cliff Sparks, and Gene Murrow are our first class organizers, and Gene Murrow (sound familiar?) and the Harvard School for providing a fine classroom facility. Also, thanks to the anonymous rich person who established a SCHOLARSHIP FUND for those who don't feel that they can afford the tuition for a class which they want to take. Thanks all.

LO*OP CENTER

LO*OP Center of Cotati, California (near Sonoma) is dedicated to three major areas of computer education; the first being a neighborhood center open to the public to teach games and problem-solving at all programming levels. The second project is to be devoted to instruction, using the computer as a tool in an educational environment in the lower school grades. Finally, LO*OP is addressing itself to the public at large through the printed media, acting as a publishing exchange of information currently on hand in the computer community.

Anyone can join the LO*OP Center. For more information call (707) 795-0405, or write 8099 La Plaza, Cotati, California 94928.

SAN FERNANDO VALLEY CHAPTER START-UP

A preliminary meeting of SCCS members to begin a San Fernando Valley chapter of the Southern California Computer Society was held Wednesday, January 7th, headed up by pro tem leader, Jerry Silver.

COURSE/WORKSHOP PROPOSAL FORM

Yes, I, ______________________ (your name) ,am OVERJOYED at the prospect of leading an SCCS class or workshop. You can reach me at ______________ (area code/phone), or ______________ (area code/phone), and my address is ______________________________

Tentative course title: ______________________________

Brief description ______________________________

____

____

Prerequisites: ______________________________

____

Number of meetings: ______ Duration of each meeting: ________ Estimated cost of materials: $ ______

Send this form and 2 MITS boxtops to: Larry Press
128 Park Place
Venice, Calif. 90291

What ensued that evening at 7:30 was an energetic conclave of home computer enthusiasts that filled the Avco Savings meeting room with a wide range of talent, from computer hobbyist newcomers to specialized professionals in all aspects of the computer community. Discussions on newly launched projects were electric and plans are now in progress to combine efforts for an entry in the WAAC (Altair Convention) competition.

Unlike the overwhelmingly large (and getting even larger) general monthly SCCS meetings, this more informal and intimate atmosphere enabled the 50 or so participants to interact, discuss and plan. A temporary committee was formed to channel proposed projects until a formal election is held. For those interested in becoming involved in a chapter close to home, the first formal meeting will be held at the Harvard School Cafeteria, 3700 Coldwater Canyon, North Hollywood on Wednesday, February 4th at 7:15 pm.

This pioneer chapter is expected to become a prototype for subsequent chapters in Southern California, and perhaps nationally.

CALIFORNIA COMPUTER SHOW FEBRUARY 19

Norm De Nardi's California Computer Show will be held at the Royal Inn in Anaheim February 19 from 1 to 7 pm and will feature the latest OEM and END-User computer systems and products.

The Orange County California Computer Show will feature 40 exhibitors showing their latest equipment. All products will be operational for demonstration. Complimentary cocktails will be served and invitations may be obtained by contacting: Norm De Nardi Enterprises, 95 Main Street, Los Altos, California 94022 (415) 941-8440.

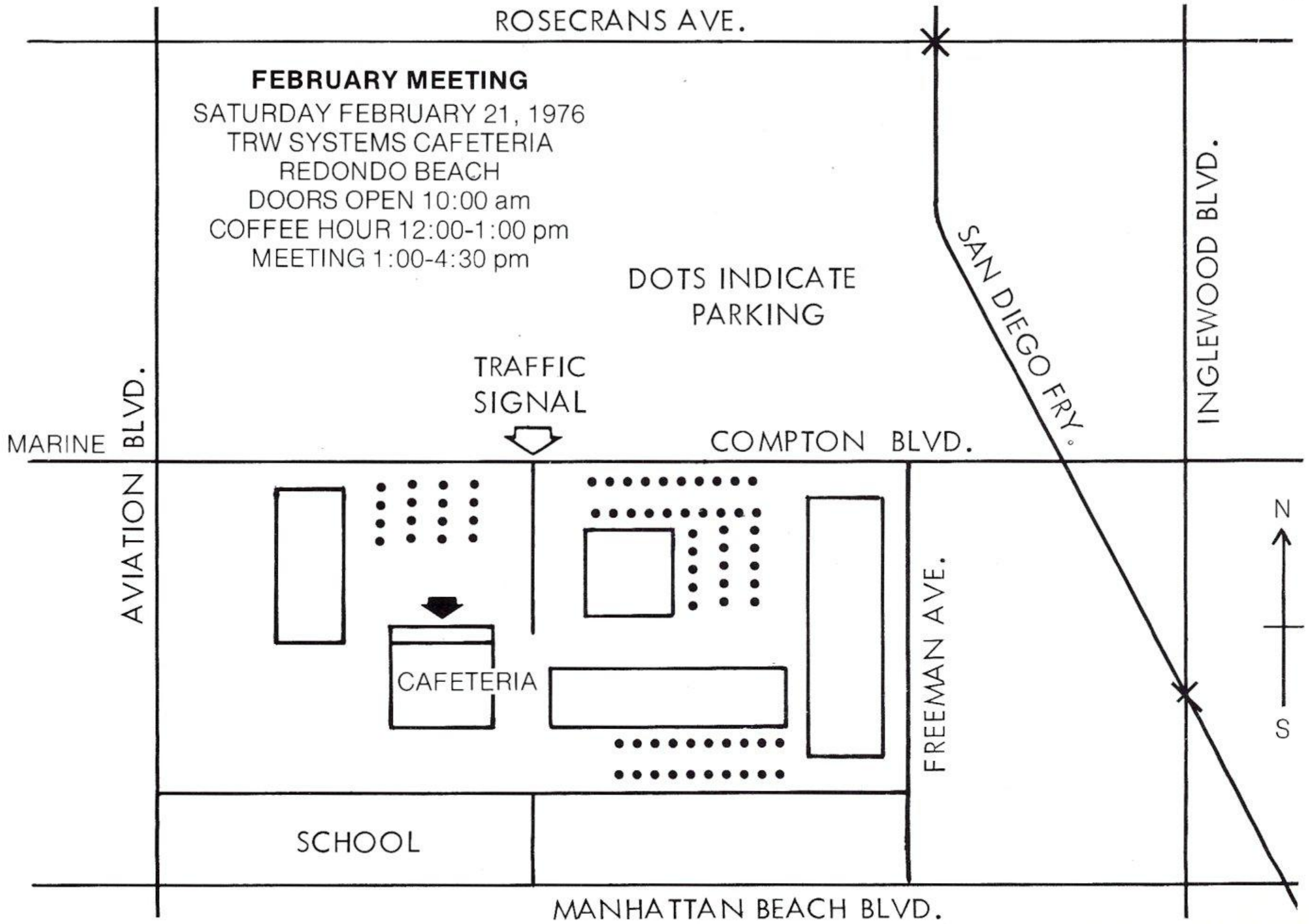
ATTENTION ALL SCCS/TRW EMPLOYEES

TRW Civic Affairs has asked me for a readout on how many TRW employees are SCCS members. I think a good response will be beneficial to us for TRW support. Please provide me with the following information: NAME, BUILDING/MAIL STATION; TRW OPERATING GROUP (Systems, Electronics, Credit Data, etc.); DIVISION, POSITION or TITLE. Also indicate if there is any specific item you want to remain confidential and I will keep it so. Send the information to:

At TRW Systems	or	At Home
R. Keele		Ron Keele
M1/1226		9823 Redfern Avenue
		Inglewood, California 90301

1976 COMPUTER SHOWS
2/19/76 ANAHEIM
4/22/76 PALO ALTO
5/27/76 HOUSTON
BOSTON
10/21/76 LOS ANGELES
12/2/76 PALO ALTO

Causing a lot of attention at a recent show was Mellennium Information System's message board, an excellent example of the use of a microprocessor in a highly visible application. Here the device displays the 1976 expanded schedule for Norm De Nardi's Computer Shows. The sign can show animation as well as the standard flashing and scrolling messages and graphics.



FEBRUARY MEETING

SATURDAY FEBRUARY 21, 1976
TRW SYSTEMS CAFETERIA
REDONDO BEACH
DOORS OPEN 10:00 am
COFFEE HOUR 12:00-1:00 pm
MEETING 1:00-4:30 pm

DOTS INDICATE PARKING

THE COMPUTER MART

One — stop computer supermarket.

STOP LOOKING all over the country for supplies and accessories for your personal computer.

We are the place to shop for:

- PROCESSOR TECHNOLOGY — Memories, Video Modules, I/O boards, etc.
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INTRODUCTION TO MICROPROCESSOR TECHNOLOGY

From "Introduction to Microprocessors" reprint courtesy of Motorola Semiconductor, Phoenix, Arizona.

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First part
Introduction to computers

Chapter V

THE BINARY SYSTEM

This chapter is intended to demonstrate the principal ideas relating to numerical systems and to binary arithmetic.

1. The decimal and binary systems of numbers

Every computer must be able to represent numbers and carry out operations on the numbers thus represented.

From childhood man becomes accustomed to representing quantities in the decimal system, that is, in a system said to be "of *base* 10"; the digits of this system run form 0 to 9; by giving these digits different positions or *"weights"* it is possible to represent numbers greater than 10.
In the general case of a system of base b, the successive positions of the digits, from left to right, have the following weights:

$$\ldots b^3\, b^2\, b^1\, b^0 \,.\, b^{-1}\, b^{-2} \ldots$$

The symbol " . " (radix point) separates the integral part from the fractional part of the number.
A computer uses the system of base 2 (binary system) rather than base 10 simply because most physical systems have only two alternative states (in particular, the digital components of the computer).

Binary-decimal conversion

The decimal value of a binary number is obtained by multiplying each bit by its weight and adding the products.

Example:

$$1011.10 = 1x2^4 + 0x2^3 + 0x2^2 + 1x2^1 + 1x2^0 + 1x2^{-1} + 0x2^{-2} = 19.5$$

Decimal-binary conversion

This is best explained by means of an example: we will convert the decimal number 53.5625 into binary notation. The integral part is converted by successive division by 2 and the fractional part by successive multiplication by 2.

$$\begin{array}{c|cl} & & \text{Remainder} \\ 2 & 53 & \rightarrow 1 \\ \hline 2 & 26 & \rightarrow 0 \\ \hline 2 & 13 & \rightarrow 1 \\ \hline 2 & 6 & \rightarrow 0 \\ \hline 2 & 3 & \rightarrow 1 \\ \hline 2 & 1 & \rightarrow 1 \\ \hline & 0 & \end{array} \Big\uparrow \quad (53)_{10} = (110101)_2$$

$$\begin{array}{llll} & & & \text{Carry} \\ 0.5625 & x\ 2 = 1.1250 & \rightarrow & 1 \\ 0.1250 & x\ 2 = 0.250 & \rightarrow & 0 \\ 0.250 & x\ 2 = 0.500 & \rightarrow & 0 \\ 0.500 & x\ 2 = 1.000 & \rightarrow & 1 \\ 0.000 & x\ 2 = 0.000 & \rightarrow & 0 \end{array} \Big\downarrow \quad (0.5625)_{10} = (.10010)_2$$

Finally: $(53.5625)_{10} = (110101.\ 10010)_2$

2. Representation of numbers

Assume that the memory of the computer is organized in bytes of 8 bits.

2.1. *Values without signs*

With 8 bits it its possible to represent a quantity by a binary number between 0 and 11 111 111 = 377_8 (see octal system, part one, Chapter VI, 2.) or, in the decimal system, between 0 and 255_{10}.

2.2. *Values with signs*

By convention, the bit 7 or MSB is taken to represent the sign of the quantity of which the value is indicated by the bits 0 to 6.

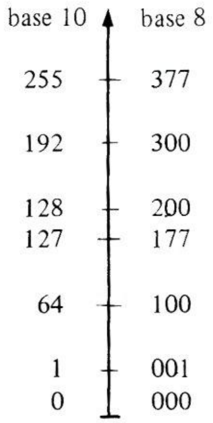
In general:

MSB = 0 for positive numbers

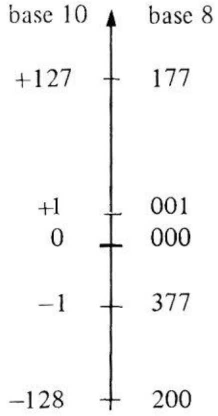
MSB = 1 for negative numbers

The highest positive number will be 01 111 111 = $177_8 = +127$

The highest negative number (in absolute value) will be 10 000 000 = $200_8 = -128$.



Values without signs



Values with signs

2.3. *Two's complement*

This notion is used for the representation of negative numbers; it is therefore only meaningful for values with a sign.

To represent a negative number it is only necessary to observe the following rule:
a) represent the absolute value of the negative number in pure binary notation;
b) invert all the bits (complement with respect to 1);
c) add 1 to the LSB.

Example: $-14_{10} = ?$
a) $14_{10} = 00\ 001\ 100_2$
b) $14 = 11\ 110\ 011_2$
c) $-14_{10} = 11\ 110\ 100_2$

3. Binary subtraction

Any binary subtraction A − B may be reduced to the addition of the number (−B) to A.
To obtain the number (−B) it suffices to take the two's complement of B (see 2.3).

Examples: $16_{10} - 4_{10} = ?$
$-4_{10} = 11\ 111\ 100_2$

$$\begin{array}{lrl} \text{hence} & 16 & 00\ 010\ 000 \\ + & -\ 4 & 11\ 111\ 100 \\ & 12_{10} & 00\ 001\ 100 \end{array}$$

4. The BCD code (Binary Coded Decimal)

The BCD notation is hybrid notation in which each digit is replaced by its pure binary equivalent in 8421 code (on 4 bits).

Example: $93_{10} = (1001\ 0011)_{BCD}$
conversely, $(0100\ 0110)_{BCD} = 4 \times 10^1 + 6 \times 10^0 = 46_{10}$

5. Floating point representation – Precision

On 8 bits it is possible to represent $2^8 = 256$ numbers. The maximum precision which it is possible to obtain in a calculation is therefore 1/256.

When it is decided to represent a number by a single word it is said to be represented in *single precision.*

If the precision obtained is not sufficient, representation in multiple precision may be used, with the number stored in several words.

There is also another way of representating numbers: this is the *floating point* notation in which the mantissa and the exponent of the number are distinguished.

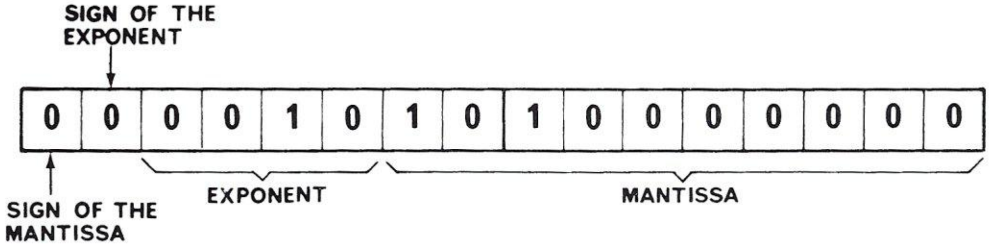
In the notation, every number N is broken down into two parts – the mantissa M and the exponent E with values such that $N = M \cdot b^E$; b is generally chosen equal to 2 and E is chosen in such a way that the mantissa M represented in fixed point contains the greatest possible number of significant digits.

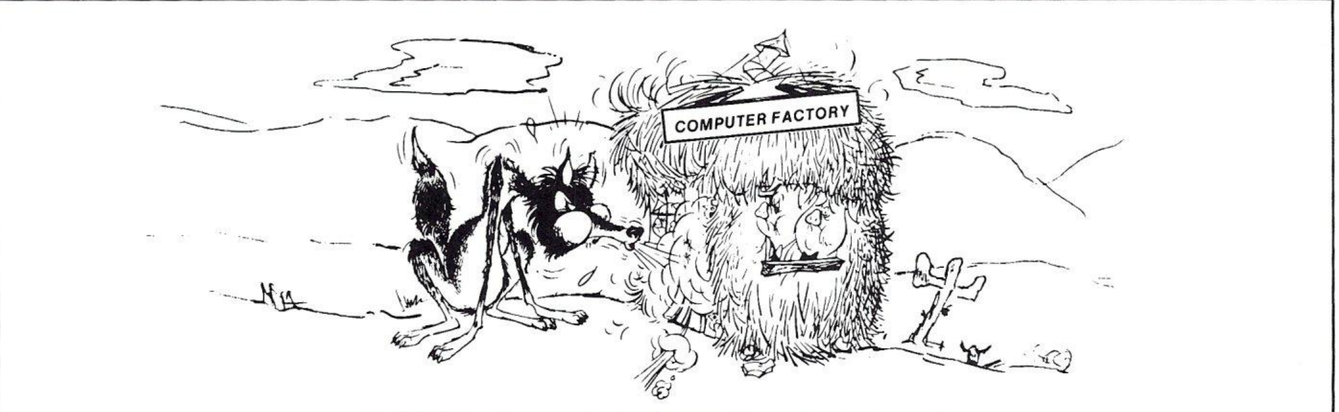
Example: representation of the number + 2.5.

We assume that all numbers are represented on 2 bytes in which 4 bits are reserved to quantify the exponent and 10 bits for the mantissa.

$$\begin{aligned} 2.5_{10} &= 010.100_2 \\ &= 001.01000_2 \times 2 \\ &= 000.1010_2 \times 4 \end{aligned}$$

Finally: $2.5_{10} = 0.101000 \times 2^2$





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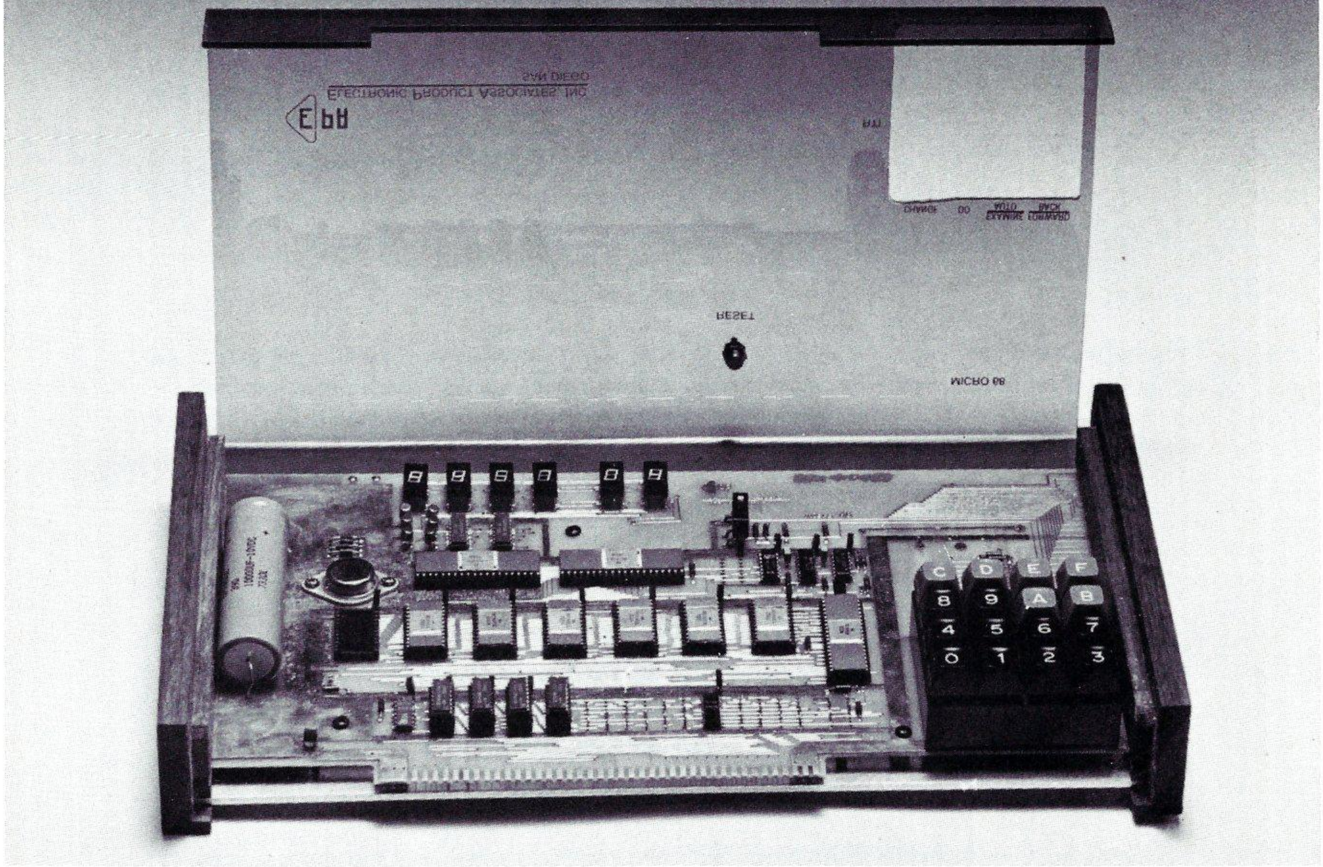

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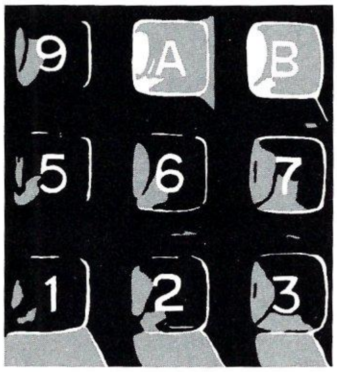

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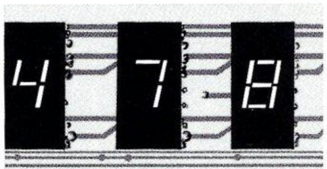

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Chapter VI

CODING—LANGUAGES

All the information in a computer is stored in binary form. However, when a programme is written, this information may be coded in a more practical form; in general, a programme may be coded in four ways which, in decreasing order of complexity, are: binary, octal, hexadecimal and symbolic codes.

1. Binary coding

This is the only one understood by the computer.
Example: On the mini-computer PDP11 from Digital Equipment Corp., the instruction CLEAR 64, which sets to zero the contents of the address position 64, is coded on 2 words of 16 bits in the following way:

CLEAR 0 000 101 000 011 111
64 0 000 000 001 000 000

It is apparent that this method of coding requires a great deal of patience and a programmer who must know the codes of each instruction could not memorize them in this form. For this reason, the octal or hexadecimal forms are generally preferred but it must be stressed that they only facilitate the writing of the programme and are not understood by the computer which only knows the binary code.

2. Octal coding

In this code, each group of 3 bits, starting from the right, is translated into octal code. The instruction, CLEAR 64, in octal code, is:

CLEAR 0 05037
64 0 00100

$$\text{Example:}\quad \text{CLEAR}\quad \underbrace{0}_{0}\quad \underbrace{000}_{0}\quad \underbrace{101}_{5}\quad \underbrace{000}_{0}\quad \underbrace{011}_{3}\quad \underbrace{111}_{7}\quad \begin{matrix}\text{(binary)}\\ \text{(octal)}\end{matrix}$$

$$64\quad \underbrace{0}_{0}\quad \underbrace{000}_{0}\quad \underbrace{000}_{0}\quad \underbrace{001}_{1}\quad \underbrace{000}_{0}\quad \underbrace{000}_{0}\quad \begin{matrix}\text{(binary)}\\ \text{(octal)}\end{matrix}$$

3. Hexadecimal coding

From the right, the binary number is divided into groups of 4 bits; each of these groups is represented by its decimal equivalent if the decimal value is less than 10, otherwise by a letter from A to F.

Group	*Decimal value*	*Hexadecimal code*
0000	0	0
0001	1	1
.	.	.
.	.	.
.	.	.
1001	9	9
1010	10	A
1011	11	B
1100	12	C
1101	13	D
1110	14	E
1111	15	F

Example: CLEAR $\underbrace{000}_{0}\ 1\underbrace{010}_{A}\ 0\underbrace{00}_{1}1\ 1\underbrace{111}_{F}$ 0A1F

4. Symbolic or mnemonic coding

The octal and hexadecimal codes represent a certain simplification relative to binary coding. However, they are still rather tiresome for long programmes. To simplify the job of the programmer, he is provided with a symbolic coding system where each instruction is represented by a group of 3 or 4 letters chosen so as to suggest the definition or function of the instruction. Thus, ADD is used to signify the operation of addition, CLR the operation of setting to zero, etc.

Although highly evocative, symbolic coding can not be understood by the computer which acts only on binary information. It is therefore necessary to translate the symbolic programme designated *"source programme"* into a binary programme designated *"object programme"* or programme in *"machine language"* executable by the computer. In practice, this translation is done by a special programme called the *"assembler programme"* which translates every symbolic instruction into its binary equivalent. The translation phase is called *"assembly"*.

5. Elementary and high-level languages

We have just looked at the languages described as elementary, namely, in decreasing order of complexity:

- – Machine language (binary, octal or hexadecimal coding)
- – Symbolic language (mnemonic coding).

There also exist languages described as *"evolved* or *high-level"* which are much easier to learn; these are languages such as BASIC, FORTRAN, ALGOL, COBOL, etc.

(Continued on page 42)

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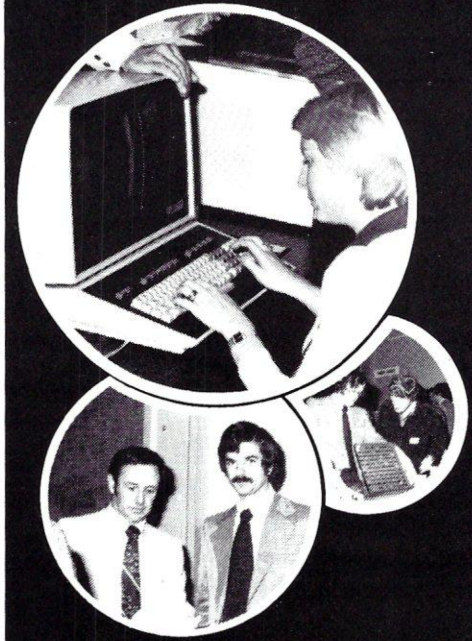

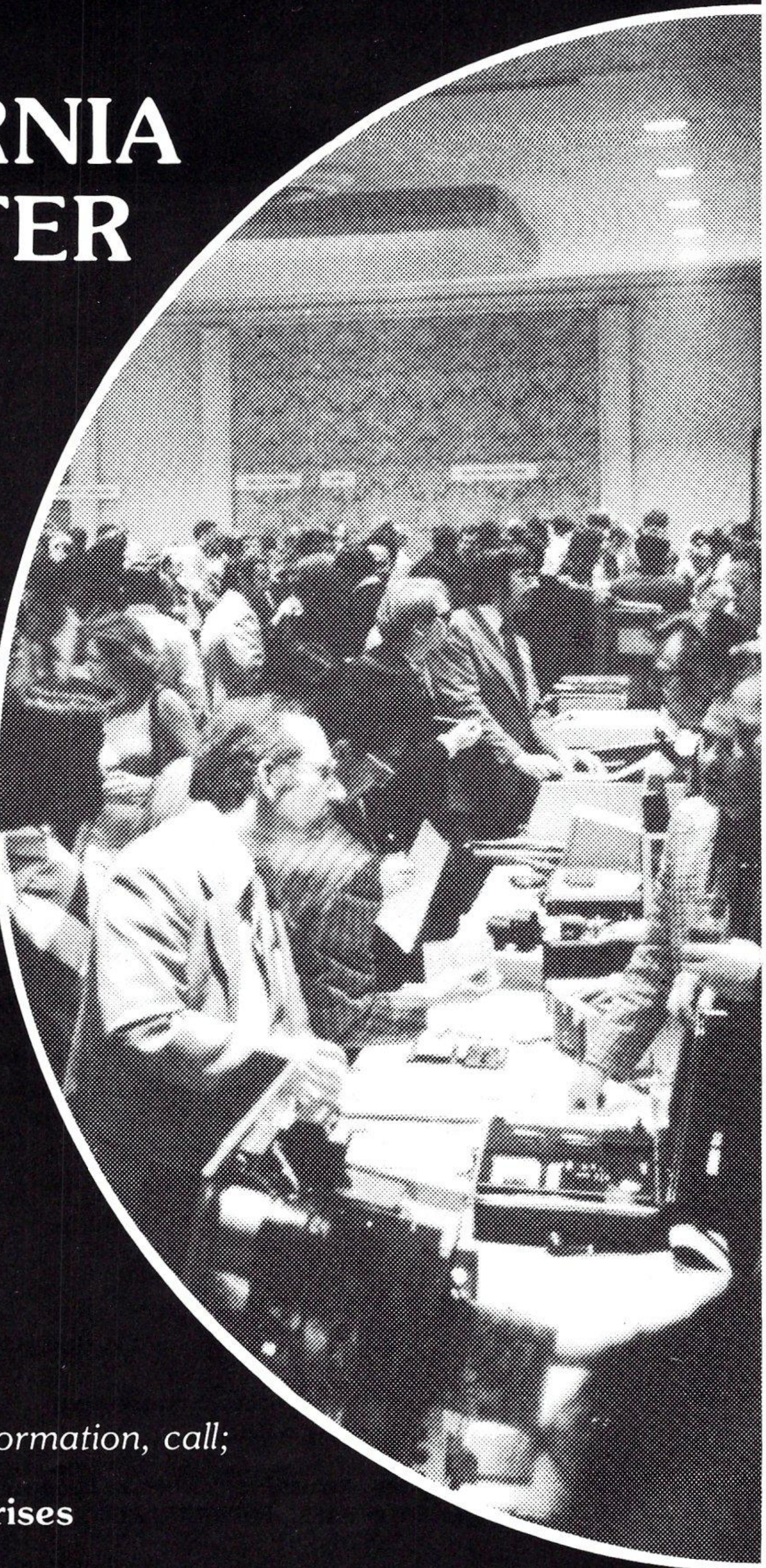

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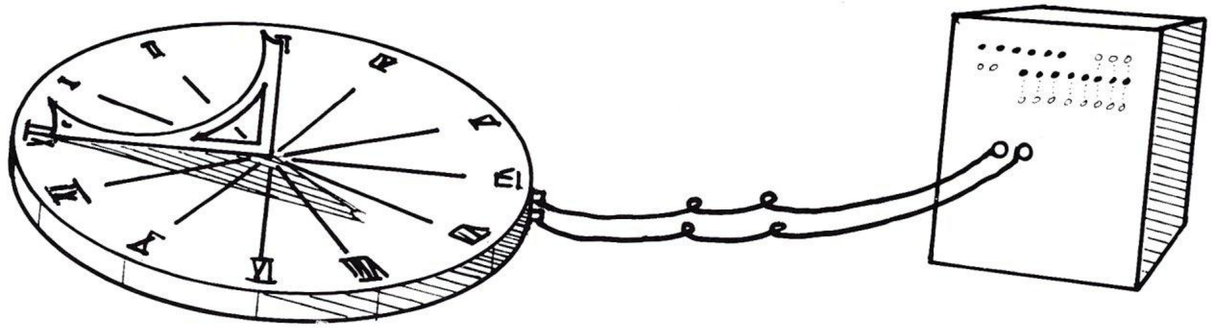


by Jerry Benson
Field Applications Engineer, Intel Corp.

Timing by Use of Microcomputers

In this series of application articles I will describe methods of using microcomputers and techniques of applying programs to logic functions. The purpose of these articles is to educate and inform those potential microcomputer users who are unfamiliar with computers or programming techniques. In most discussions, it will be supposed that the reader has some knowledge of logical operations and consequently much of the hardware interface will be abbreviated.

In each application of programmed logic (sometimes referred to as software), the program philosophy, flow and features will be discussed. A complete program description will be provided. First at a general level, then at a more detailed specific level.

As a preface to describing how to effect logical operations, it should be understood that in many cases, one program instruction will replace the function of a standard logic element — such as an AND gate. A corollary of this statement would suggest that to duplicate the function of say, a flip-flop, it would take at least two logical statements. As we progress through this month's application example, we will see an indication of this "replacement" function — that is, to directly replace logical functions with logical program statements.

A TIMING FUNCTION

In order to begin programming any application, a flow chart should be generated. A flow chart is analogous to a block diagram used to describe hardware functions. The flow chart is used to define the steps — or logic functions — to be performed in the program. Various symbols may be used to express different types of operations, while the exact operation is described within each symbol or block. The flow chart is used to define the required operations and at the same time simplifies the process of revising the program.

DEFINITION OF TASK

The task of this example is to develop a program that sets up a timing sequence to generate a pulse at predefined intervals.

FLOW CHART (Refer to Figure 1)

The first block of the flow chart indicates that a counter is to be set to a predetermined value. This value is required for operation in the program to develop a pulse train with known period. The actual value of the counter will be determined after completely formulating the program. Thus, the first function to be performed is "set counter". In the second step, a pulse is formed on an output line. After completion of the pulse, the timing loop begins. This is accomplished by first verifying that the counter is not zero and then decrementing it. This sequence, or loop, is maintained until the counter reaches zero. Once the counter gets to zero, the specified time period has elapsed and another pulse can be generated. This requires that the program be executed again. We have now generated a flow chart representing the functions that our program must execute to develop the timing pulses required.

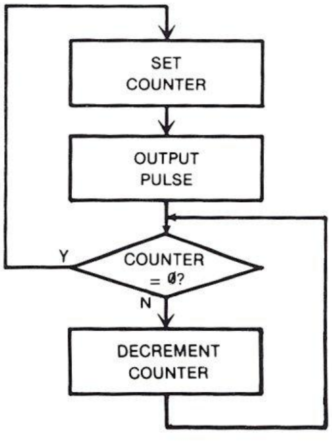


Figure 1

EXPANSION OF FLOW CHART

Figure 1 indicates the major functions to be performed for this timing application. However, it can be expanded to more completely describe the logical operations that will be executed for this task while using the 8080. You will note that the flow chart is actually tailored for the processor that is being used. (See Figure 2. The names outside of the boxes represent "labels" or names that can be reached by means other than sequential execution.)

Notice that the "output pulse" block has been expanded to show that the pulse is actually to be formed with the programmed instructions. The XRA A, exclusive or A with itself, actually clears the accumulator. In addition, since the nature of the counter is directly related to the CPU being used (8080), expansion of the counter loop can reflect the actual counting procedure.

There is a 16 bit register in the 8080 that will be used as a single 16 bit register (actually the 8 bit registers B and C are used). One of the functions provided in the 8080 instruction set decrements the 16 bit BC register (DCX B) but no flags are affected. This requires that a test of each 8 bit register be separately performed. Consequently, the flow chart has been modified to reflect the two tests — a logical 'AND':

> If both B = 0 *and* C = 0 then the loop is complete; otherwise decrement BC and check again.

The actual AND function is performed by ORing both registers together and checking for a zero condition (Do you see how we can replace logic gates?)

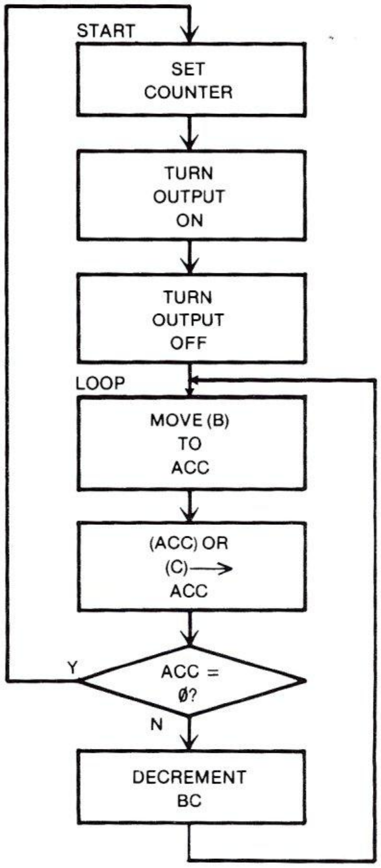


Figure 2

DEFINE HARDWARE

The output port must be specified and can be considered the address of the output data. It can be selected as any number from 0 to 255; but usually is chosen so that, with all inputs and outputs considered, the least amount of hardware will be required to decode the input-output addresses.

In this example, output port 8 will be used since only one bit in eight (00001000) need be decoded. This is one method of system optimization (sometimes referred to as "linear addressing") that can help to reduce the amount of hardware required in a microcomputer system.

Now we must define the bit that will be used as the pulse train output. Bit 1 (second bit from right) has been chosen in this example. Also, we have assumed that no other bits on port 8 are being used (N.U. = not used) during this operation. (The other 7 bits can be used but special precautions must be observed so as not to affect them when changing bit 1.) See Figure 3 for a description of the output port arrangement and the timing of the output bit.

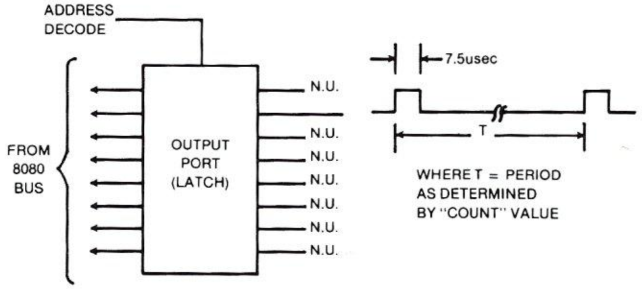


Figure 3

WRITING THE PROGRAM

The next step is to begin writing the program functions described in each element of the flow chart. (See Figure 4.) In some cases, more than one instruction will be required to complete the function. Note that two blocks in the flow chart can be reached from more than one place within the program. These blocks have been assigned labels, START and LOOP, that can be reached from more than one place within the program. These labels are arbitrarily assigned but should be mnemonic (look it up!) in nature to make it easier to write the program and also to assist in program documentation.

Each line of the program represents one machine instruction which can be converted to machine language by an "assembler". (For a small example like this, assembly can naturally be done by hand.) With each "line of code" a comment is included to describe, in English, what is occurring. These comments can, and should, be included in the final listing but in no way affect the operation of the program — hence the semicolon (;) separating the statement from the comment. Also, included in the listing is a column which lists the number of machine cycles that are required to execute each instruction. This information will be necessary to determine the exact timing cycle of this program. Each cycle requires 500 nsec (.5 usec) for the 8080 operating at a 2 MHz clock rate. This cycle information is used to determine the time required to execute an instruction by multiplying the number of cycles by .5 usec. For example, the ORA C instruction takes 2 usec while the MVI A, 2 takes 3.5 usec. (The line numbers are only included here for discussion purposes and are not required for actual program preparation.)

On line 1, the BC register is loaded with a 16 bit value designated "COUNT". "COUNT" will be set to some value just before the program is finalized so that it will determine the total cycle time. In lines 2 through 5, a pulse is generated. In line 6, the contents of register B are loaded into the accumulator. In line 7 the contents of register C are ORed with the accumulator (which contain the value from register B). If, after this operation, the accumulator is zero then both B *and* C are equal to zero. In this case we return to START to output the next pulse. However, after the OR function, if the accumulator is not zero, the BC register pair is decremented and we check again for zero in B and C.

SUMMARY

I feel it is safe to say that the program as shown will run forever. In fact, if the program were implemented as shown, the CPU would spend all the time in this loop and no other activity could take place. This program, if properly implemented in a larger program, can be used to generate program delays or to time external events, as long as there is an exit point — perhaps instead of going back to START.

Until next month, I would like to suggest that you evaluate the timing function of this program and calculate the following parameters:

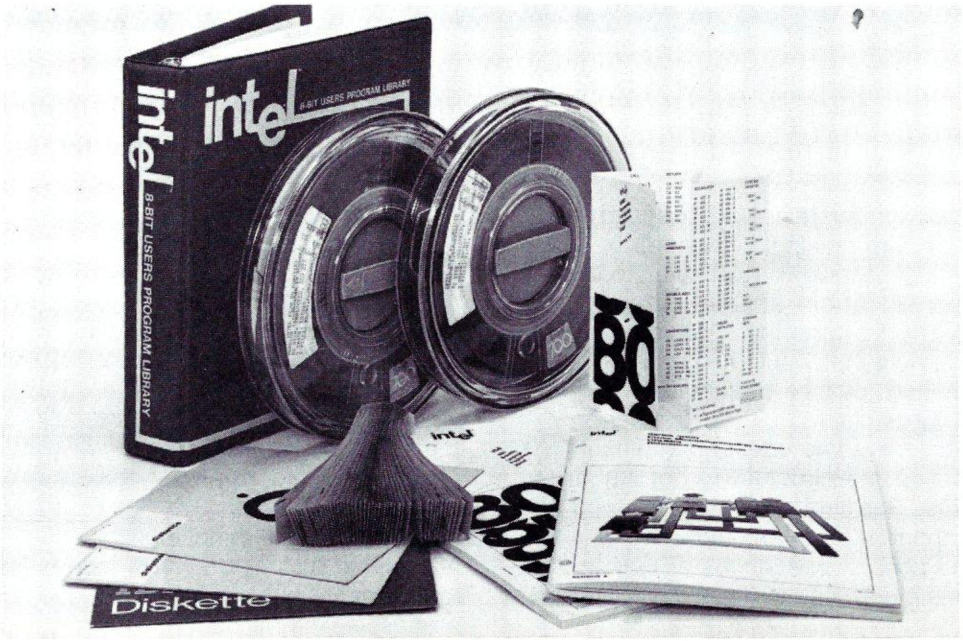
1) Determine how long the cycle will be if COUNT = 0;
2) Determine how long the cycle will be if COUNT = 65535 (all 1's);
3) Determine what value of COUNT would be required to generate a 4.55 msec time period.

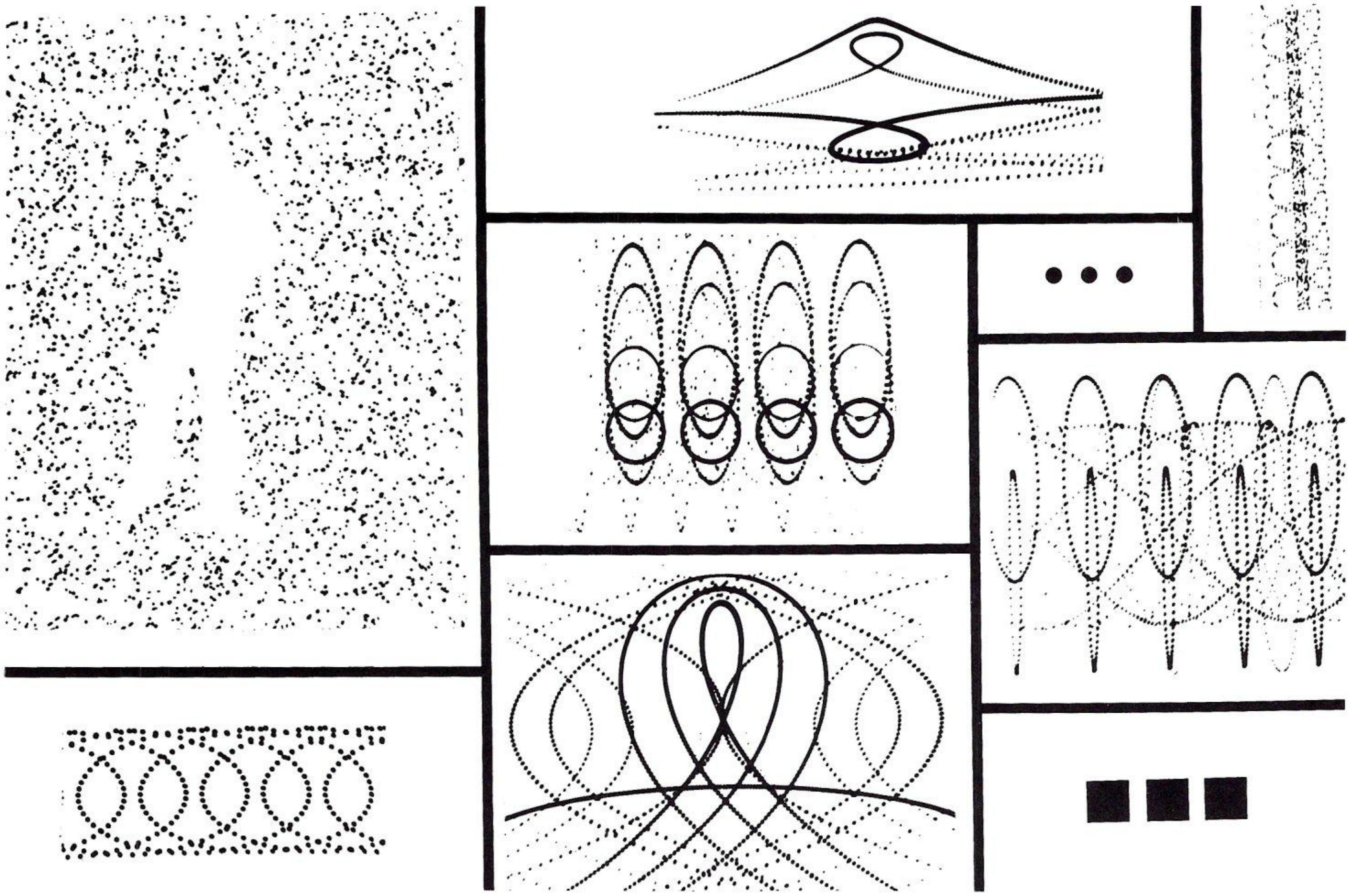
You might also modify the program to generate a square wave output instead of the pulse as shown. (Note that the pulse generated in this example will last for 7.5 usec.)

Next month a solution for each of the above "homework problems" will be provided. I will also discuss the usefulness of flow charts for modifying programs. The main topic for the next application will show how to make use of the timing technique discussed in this article to create a serial transmit and serial receive subroutine for teletype, or other similar input-output communication device. This will allow communication to a TTY without the use of a UART — if you really want to reduce hardware.

```
Line No.   Cycles   Label    Operation      Comments
   1         10     START:   LXI B, COUNT   ;LOAD BC WITH COUNT VALUE
   2          7              MVI A, 2       ;USE BIT 1 (00000010)
   3         10              OUT 8          ;OUTPUT CONTENTS OF A TO PORT 8
   4          5              XRA A          ;CLEAR A
   5         10              OUT 8          ;OUTPUT TO PORT 8
   6          5     LOOP:    MOV A,B        ;GET HIGH ORDER 8 BITS
   7          4              ORA C          ;OR WITH LOW ORDER 8 BITS
   8         10              JZ START       ;IF ZERO, GO TO NEXT PULSE
   9          5              DCX B          ;DECREMENT 16 BIT COUNTER
  10         10              JMP LOOP       ;GO CHECK FOR ZERO
```

Figure 4





FURTHER REFLECTIONS OF A CULTURE SAVAGE

by John Whitney

When I ask what hardware would best serve my kind of computer art film making, I find that there are some fairly practical answers available today — answers which do not strain state-of-the-art, 1976 availability of electronic graphics. Indeed there is hardware available now that would just about replace my expensive motion picture machinery and the perforated silver ribbon itself.

I will try to present some ideas that should be influential in planning instrumentation for an art of computer dynamics. This kind of electronic sound and image is a wide-open field and should interest many newcomers for its special challenges as well as for the rewards of tangible results from programming effort.

First let me remark that I disown my profession; I am a filmmaker of necessity — not by choice. I have waited a long time for this day when the irrational and damnable perils of film making would disappear. Everyone who has worked with film, amateur and professional alike, knows the heartache that comes after extensive and expensive effort is committed — when at the final juncture the lab informs its victim that one of a thousand unpredictables has occurred and his film is ruined. This happens repeatedly because the rupture of the feedback message is absolute. With filmmaking the chasm between artist and all his best effort is as deep as oblivion until the fateful moment his lab man hands back the fixed and processed roll of film.

But now let us put all that behind once and for all. We stand at a moment when, for the first time, we may deal with a dynamic, ephemeral visual art medium almost as if it were clay in our hands; to be molded and shaped and reshaped in a fairly well-closed feedback loop. Here are some ideas about that.

It would be sensible to display computer graphic output on a standard color video since color TV is already the world's greatest and cheapest unexplored color device. I say unexplored because in fact, we may never fully explore the limits of the video phosphores for their latent color saturations and intensities.

Color TV, as it is used today, is programmed to reproduce honestly only those particular colors that make up the world. If the sky is blue, the electronics engineer tunes the TV camera and picture tube to convey to us exactly **that blue.** Only if we interfere with the normal system and deliberately mistune the set, will we get the kind of blue colors which are actually possible with the phosphores. Thus, if we make a fine art of these deliberate false tunings, we may synthesize, create, or man make new and astonishing color experiences . . . experiences that have never before been possible, because the video phosphores can generate color better than pigments or dyes or color film, or anything the eye has ever seen.

Next, we must have a way to capture and hold all these unprecedented color miracles we shall produce with our special computer graphics. In the first place, probably no microprocessor can generate our kind of pattern in real-time. We must allow the graphic equations to be computed picture for picture. Perhaps it will take six to twenty seconds per frame. So let us store the vector or picture data of this processing on a floppy disk. That is, let us accumulate the data for a total of about a ten-second sequence. The disk can hold this ready to replay in real-time on the color video display.

Next we may output from disk to video display in real-time. We may view and evaluate this display. If corrections are needed, we return to the processor, regenerate and store the new computations on disk. Then play back, evaluate once more, and proceed.

This is the closed feedback loop referred to earlier. Step by step, we can evaluate and correct, thanks to the erasability of magnetic storage media (photo storage just won't do). Our instrumentation will have the feel of clay or marble, according to how well we are able to facilitate each part of the full circle loop at these operations.

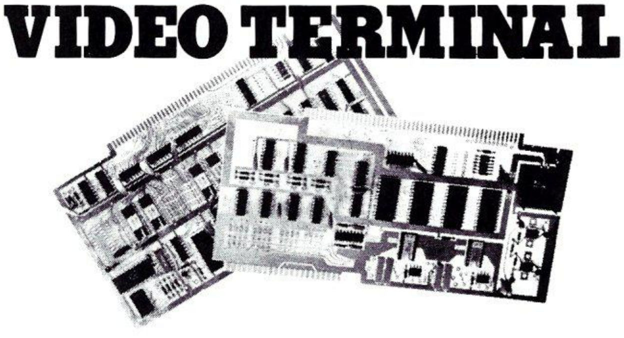
A floppy disk will probably hold only one ten-second sequence at a time. What should we do if we want to string many ten-second sequences together? We have at hand, ready on the shelf and waiting for our use, the video tape recorder. Why not design interface hardware and software to provide a direct hookup between disk and VTR? This black box link between disk and VTR should provide sync lock features so that a series of ten-second sequences from disk could be strung together or superimposed, one at a time, for uninterrupted continuity at playback.

A final comment: we cannot avoid objections about picture resolution with video standards being as poor as they are. These objections are best dispelled by suggesting a look at some traditional visual art materials. We need only consider etched copper and the lithographer's stone to realize that visual media come in all degrees of resolution, just as they come in all colors. We need not stumble because we have not invented the ultimate universal visual media. There is much to be created with even a "fuzzy" television image if the design is fresh and the action is alive.

All the above is essentially the imaginary machine that was conceptualized over several visits with Professor Herbert Baskin, at the University of California Berkeley Computer Science Department. We are tentatively planning to urge the prototyping of such a system for a research project for some members of the Berkeley Campus Computer Science community. But what could we do with it in Southern California? Aren't there talents in the SCCS who are willing and interested to take on a similar design and prototyping task as a special interest group project within our computer society? I hope so.

Of course, there is much more to write about regarding the visual dynamic and aural problems and how they must relate to hardware. This much must serve as a preface to which more will follow, chapter and verse. ◻

ALTAIR 8800
VIDEO TERMINAL



Video Interface. Plugs into the Altair or IMSAI 8800 bus and connects to standard TV monitor (or modified receiver). 8-bit input connects to almost any keyboard. Characters are displayed as 16 lines of 64 or 32 characters each, in a 7x9 dot matrix. (64 character line requires a high resolution monitor or extensively modified receiver.) The character set includes 128 upper and lower case ASCII characters and 64 graphics characters for plotting a 48x128 (or 64) grid. Characters are stored in the onboard memory and may be accessed directly by the computer. The output is standard 525 line EIA RS170 video.

$160 Kit $230 Assem. and tested (Add $25 for 64 character option) delivery 30 days

Micro Computer. A one board computer system containing an 8080 processor, 512 bytes RAM, space for 1-3 K bytes PROM or ROM, and a serial I/O port (optional). Compatible with IMSAI and Altair memory and peripherals. Supports multiprocessing. (Avail. 1st Q. 1976)

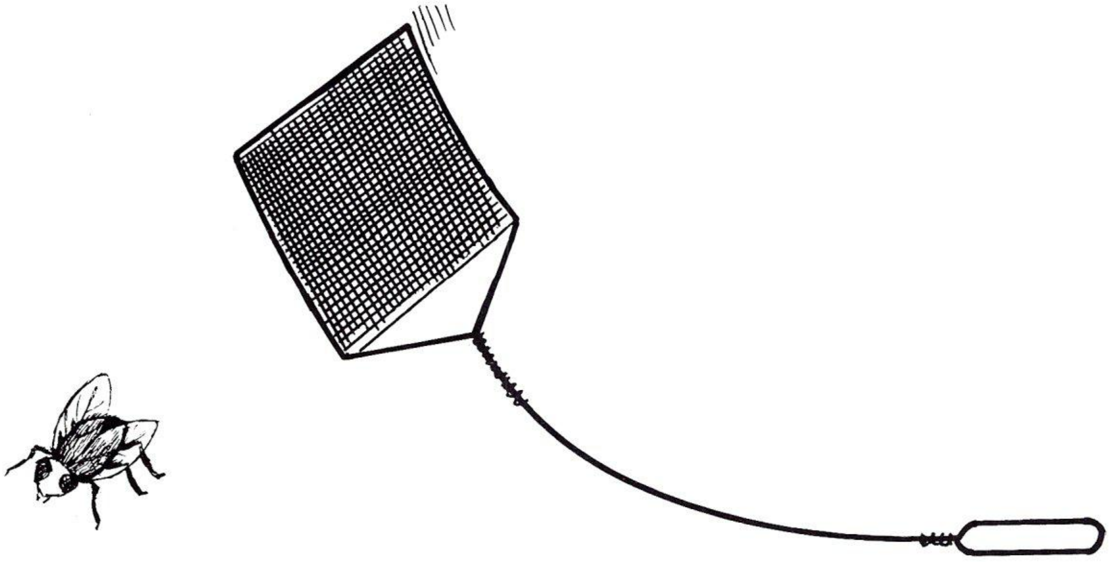
Analog Interface. This board is a complete interface for a CRT graphics display or an X-Y plotter, and provides 8 channels of software-controlled A/D conversion. There are 1 or 2 channels of analog output with 10-bits resolution (0-10v or ± 5v out), 6-bits of latched digital output, and 8 analog comparators.

1 channel (0-10v): $135 Kit $175 Assem. and tested, 2 channels (0-10v): $185 Kit $235 Assem. and tested, (Bipolar option (± 5v) add $8 for 1 ch., $12 for 2) delivery 30 days

Microcomputer System. A system based on our microcomputer and video boards. Includes motherboard, cabinet, power supply, and an operating system and monitor on PROM. (Avail. 1st Q. 1976)

All prices and specifications subject to change without notice. Prices are USA only - Calif. res. add 6% sales tax.

POLYMORPHIC SYSTEMS
P.O. Box 2207, Goleta, California 93018



Bug Chaser

by Lorne Douglas

The following routine, contributed by SCCS member Lorne Douglas, can be a very useful 8080 assembly language program debugging tool. A call trace instruction inserted at any location in the program to be debugged will cause the address of the instruction after the call to be printed on the output device, as well as the contents of all the registers just prior to the call.

Subroutines X, Y, Z and CRLF have been omitted as they are directly involved with system I/O configuration which may vary from system to system. Subroutine X merely outputs one ASCII character. The character to be output will be in register C when the subroutine is called. CRLF, as the name implies, outputs a carriage return/line feed.

Subroutine Y converts the contents of an 8 bit byte to two hexidecimal characters and outputs the result. The data to be converted is available to subroutine Y in the A register. Subroutine Z merely prints a blank or space.

Many monitors have the four preceeding routines built into them, in which case the user need not re-invent the wheel by coding them. If such is the case with the monitor in the system being used, the programmer need only assure that the data to be converted and/or printed is in the register (or memory location) anticipated by the monitor routine.

To accomplish the prescribed task in a manner that is transparent to the calling program, the trace routine, immediately upon being called, saves all eight registers in the stack, as well as the contents of the memory location whose address is in the H & L registers, and the address of the trace call instruction.

After the heading line is printed all the values saved are printed, the stack pointer returned to its proper value and control returned to the calling program.

When trouble-shooting complex programs the programmer will often insert a call trace instruction at several critical points. To avoid the repeat printing of the heading each time the trace routine is called, the heading print instructions may be omitted.

USING THE TRACE ROUTINE

The trace routine may be used in any of several ways to help isolate a program bug — or to simply verify that the machine is performing in the manner intended by the programmer. By inserting the call trace instruction at a decision point such as the test of a counter in a loop, or an address comparison routine, the programmer can see the exact results of the machine logic in the status word.

By inserting a call trace instruction at the beginning of each major program branch or loop, the exact sequence followed will be displayed as the address is printed each time the trace routine is executed. By placing the call statement at the decision point, the reason the machine took a particular branch will be displayed.

This routine is also a valuable education tool to learn exactly how the machine "thinks". For example:

```
MVI A, OFH
CPI OOH
CALL TRACE
CPI OFFH
CALL TRACE
```

By checking the status word (designated "F" in the trace routine heading) at each of the call trace instructions, the condition of the sign, carry, auxiliary carry, zero and parity bits and the way they are affected by the CPI operations becomes apparent.

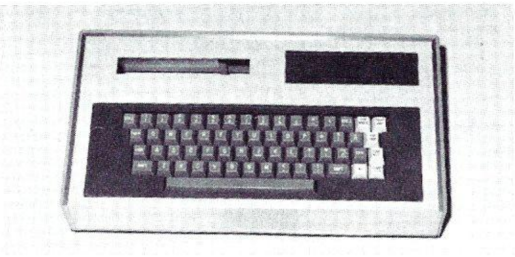
```
     HEAD   EQU $      ;HEADER
2A542A20                    DB  '*T* A F   B C   D
20412046
20204220
43202044
20452020                    DB  ' E   H L   M    SP'
48204C20
204D2020
20205350
     TITCH  EQU  $-HEAD
     ;
     TRACE      EQU  $       ;  *  ENTRY
F5                                    PUSH PSW
C5                                      PUSH B
D5                                      PUSH D
E5                                      PUSH H
```

The data to be displayed is all pushed into the stack in the order of the dump.

```
46                                     MOV B,M
23                                       INX H
4E                                     MOV C,M
C5                                      PUSH B
M is considered a 16 bit location
120C00                               LXI H, OOCH
39                                      DAD SP
E5                                      PUSH H
Stack value prior to trace call
2B                                       DCX H
E5                                      PUSH H
Calling Address. Save for dump.
Now dump the trace title line.
                                     CALL CRLF
0620                               MVI B,TITCH
Number of CHR
216208                               LXI H,HEAD
CHR String
                        LOOP             LOOP:
4E                                     MOV C,M
Pick up CHR
CD8901                                  CALL X
Print it.
05                                       DCR B
CAA208                                 JZ DONE
See if done.
23                                       INX H
Address of next CHR
C39608                                JMP LOOP
                        DONE
                          ;
                          ,
CD7D01                               CALL CRLF
Next line.
```

Now that the title is printed, it's time to dump the data in the stack.

```
E1                                       POP H
Restore printer.
0607                                    MVI B 7
Byte pairs.                             LOOP2:
C5                                      PUSH B
Save count.
7E                                     MOV A,M
Pick up first 1
CD8001                                  CALL Y
Dump it.
2B                                       DCX H
7E                                     MOV A,M
CD8001                                  CALL Y
Next 1
2B                                       DCX H
CD8301                                CALL BLK
Print Z
C1                                       POP B
Loop Count.
05                                       DCR B
C2A808                               JNZ LOOP2
Test if done.
CD7D01                               CALL CRLF
New Line.
All done, now restore registers and exit.
E1                                 POP     H
E1                                 POP     H
Now in sync—restore the true H
E1                                       POP H
D1                                       POP D
C1                                       POP B
F1                                     POP PSW
C9                                         RET
                                     **ADIOS**
```



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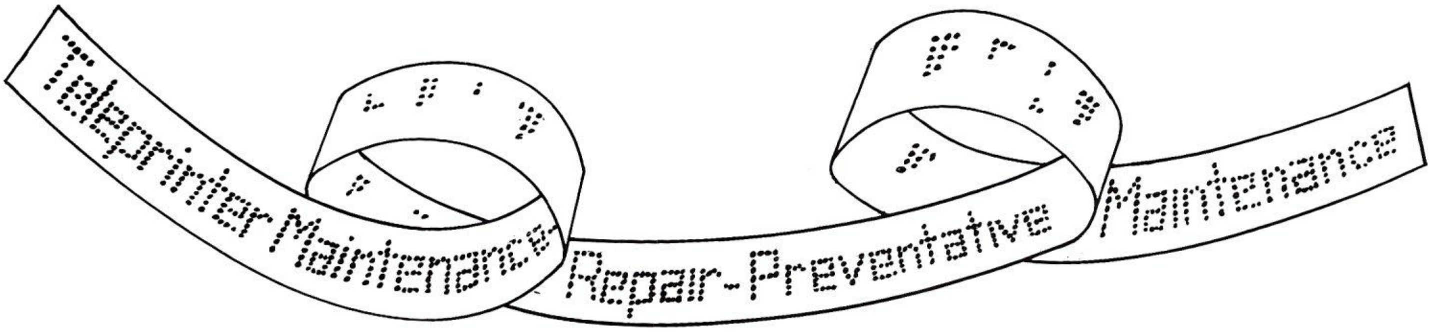

Teleprinter Maintenance-Repair-Preventative Maintenance

by Cliff Sparks

This article is the third in a series describing the operational functions of the 33ASR/KSR.

In our second article we talked about the functional groups that make up our Teletypewriter. This article will introduce the reader to the sequence of mechanical and electrical events that occur during the cycle of operation. Thru the courtesy of the TELETYPE® CORPORATION, 5555 Touhy Ave., Skokie, Illinois we have been granted permission to reproduce some of the illustrations extracted from Volume 1, 310B Manual. Many thanks to the fine folks back in Skokie for their understanding and cooperation. To start the cycle of operation, select a keytop and depress it. This action triggers the following events: (see figure 1) Selected keytop falls into slots cut out on the keyboard codebars. T levers tilt as codebars slide to accommodate selected keytop. Keyboard contact wires are moved to either a marking or spacing condition by the tilting T levers.

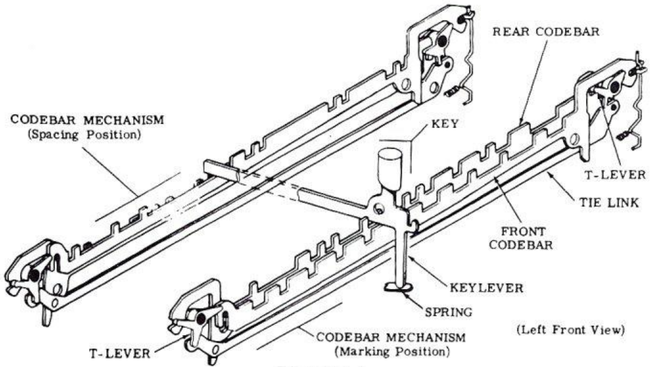
REAR CODEBAR
CODEBAR MECHANISM
(Spacing Position)
KEY
T-LEVER
TIE LINK
FRONT
CODEBAR
KEYLEVER
SPRING
CODEBAR MECHANISM
(Marking Position)
(Left Front View)
T-LEVER

Figure 1

At this point two events occur simultaneously.

MECHANICAL ACTION:

1. Selected T levers have tilted contact wires in a manner that has caused electrical impulses (Marks or Spaces) to be sent to the segments on the distributor disc. (see figure 2)

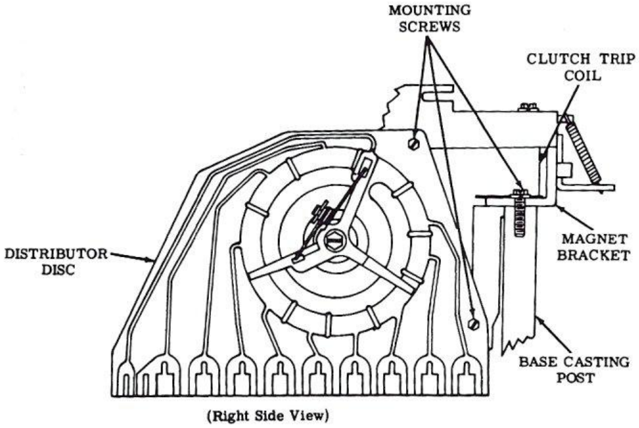
MOUNTING
SCREWS
CLUTCH TRIP
COIL
DISTRIBUTOR
DISC
MAGNET
BRACKET
BASE CASTING
POST
(Right Side View)

Figure 2

ELECTRICAL ACTION:

2. Pressing the selected keytop has caused the Universal lever to spring upward because the latch lever has been allowed to swing free, thus removing its blocking effect. (see figure 3) The electrical action caused in step 1 will be transmitted to the segments on the distributor disc.

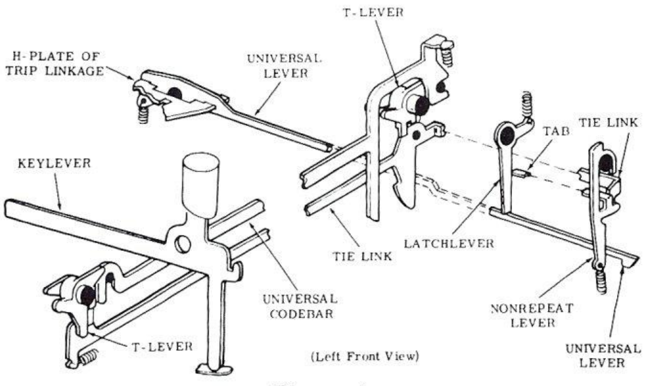
T-LEVER
H-PLATE OF
TRIP LINKAGE
UNIVERSAL
LEVER
TAB
TIE LINK
KEYLEVER
TIE LINK
LATCHLEVER
UNIVERSAL
CODEBAR
NONREPEAT
LEVER
T-LEVER
(Left Front View)
UNIVERSAL
LEVER

Figure 3

The mechanical action will be transmitted thru the Universal lever, the H plate, the distributor trip linkage, to the keyboard follower lever (see figure 4) within the distributor trip linkage area.

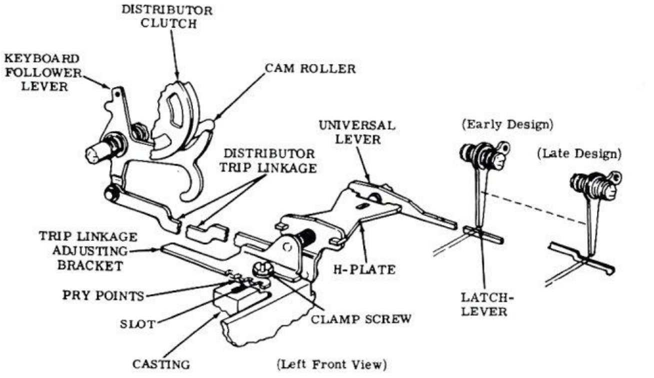
DISTRIBUTOR CLUTCH
KEYBOARD FOLLOWER LEVER
CAM ROLLER
UNIVERSAL LEVER
(Early Design)
(Late Design)
DISTRIBUTOR TRIP LINKAGE
TRIP LINKAGE ADJUSTING BRACKET
H-PLATE
PRY POINTS
SLOT
CLAMP SCREW
LATCH-LEVER
CASTING
(Left Front View)

Figure 4

The distributor clutch assembly is driven by a belt from the motor. The large belt gear is next to a clutch gear assembly that provides power to the main shaft of the printer. Next to the clutch gear is the distributor clutch assembly, then a cam assembly. Each end of the distributor shaft is mounted on oilite bearings. Attached to one end of the distributor shaft is the distributor brush holder. This is the device that sweeps a pair of contacts over the face of the segment disc. (see figure 5)

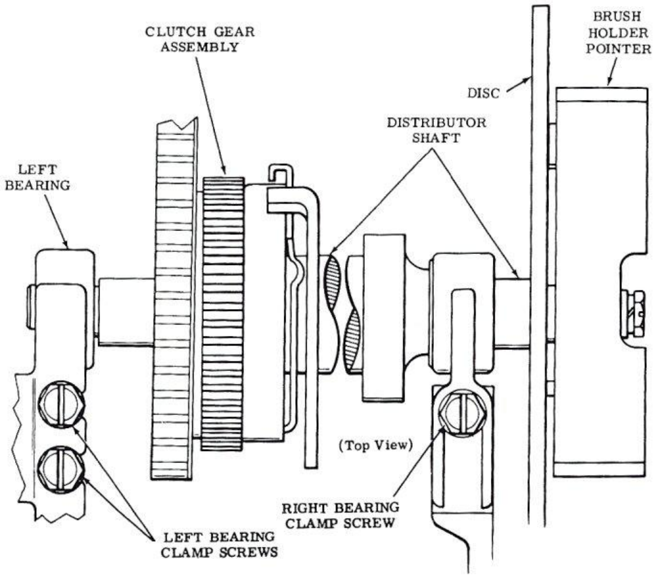
CLUTCH GEAR ASSEMBLY
BRUSH HOLDER POINTER
DISC
DISTRIBUTOR SHAFT
LEFT BEARING
(Top View)
RIGHT BEARING CLAMP SCREW
LEFT BEARING CLAMP SCREWS

Figure 5

Simply then the distributor mechanism is powered by the motor and does not move, or cause the distributor brush holder to sweep the segment disc unless the distributor clutch is tripped. How then to trip the distributor clutch? First lets look into the workings of the clutch assembly.

The clutch on the model 33 are very similar in operation and design to that of the automobile brake system. (see figure 6) When the clutch is tripped (engaged) two brake like shoes expand against a notched drum. The force of the expanded brake shoes against the clutch drum is enough to engage the drum. As the drum turns (rotates), the whole clutch and any other devices attached to it will rotate. The model 33 has four clutches and all operate in the same manner. The clutch drum is attached to and rotates with its associated shaft. When the clutch is in a stop condition the trip lever and a latch lever hold the clutch shoes, a cam disc, and a cam sleeve stationary. If the trip lever moves away from the shoes lever, the shoe lever, under spring tension, moves away from the stop lug on the cam disc.

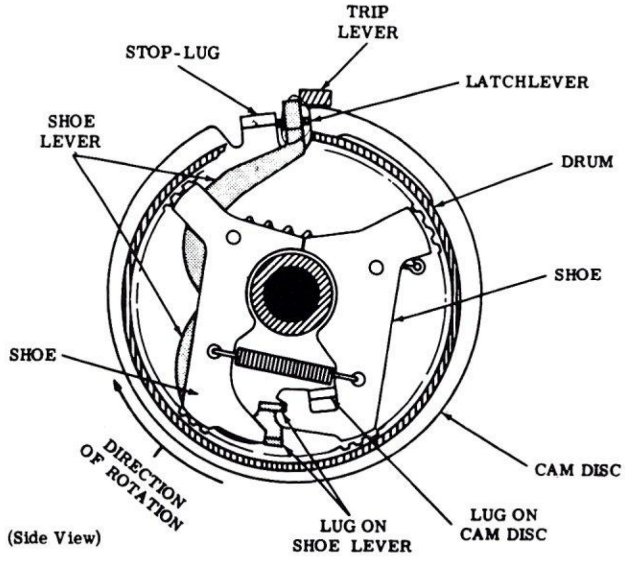
TRIP LEVER
STOP-LUG
LATCHLEVER
SHOE LEVER
DRUM
SHOE
SHOE
DIRECTION OF ROTATION
CAM DISC
(Side View)
LUG ON SHOE LEVER
LUG ON CAM DISC

Figure 6

Another approach to understanding the function of the clutch is to look at its operation and compare it to the function of the auto brake system. You may consider that the latch lever operates like a brake pedal, the trip lever as your foot, and the clutch shoes as the expanding shoes within a brake drum. Therefore if we say that a clutch is disengaged, we understand that the clutch shoes are away from the drum, so that all attached to the drum will not rotate or otherwise function.

In the case of the distributor clutch, movement of the linkage between the keyboard and the distributor trip linkage will cause the distributor clutch to trip. This engagement of the clutch will unite the entire shaft and all associated gears and cams into one rotating unit. The distributor trip linkage and the trip are under spring tension and will return to their normal position during the end of a cycle. In order to repeat the procedure another selected keytop must be pressed.

At this point we should be able to understand that just about all the major functions of the machine are under some sort of spring tension and awaiting either the pressure of your finder on a keytop or the receipt of an incoming signal from some external source. ◻

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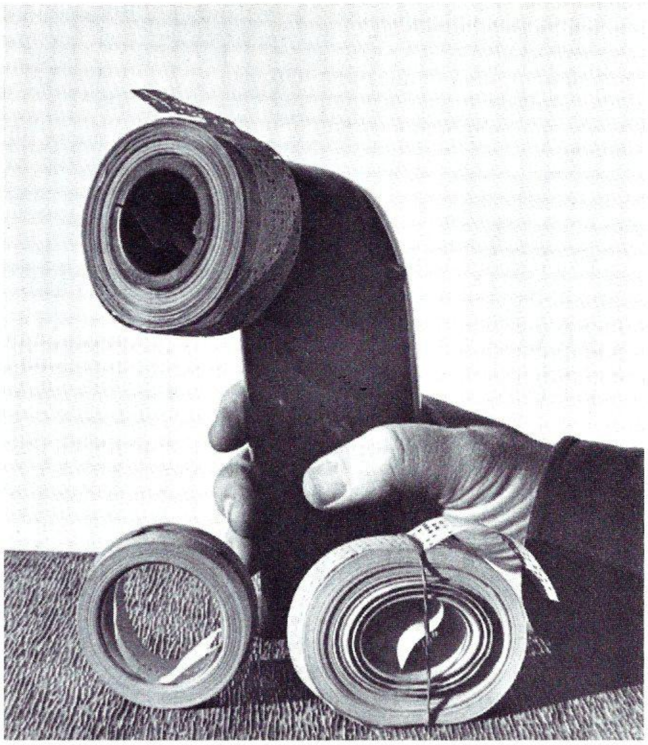
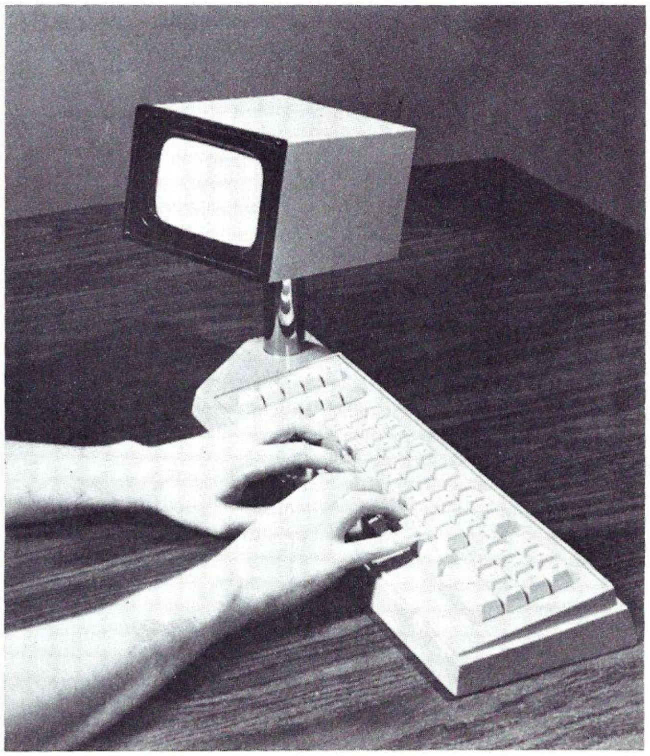
Memory-I/O options include RAM in 80 word IC and/or 1280 word PCB up to 2560 words. PROM/ROM offers storage expansion in 256 byte preprogrammed increments and/or 2K bytes or 4K bytes to a maximum of 16K bytes. I/O Options allow up to 32 ports either as 32 unidirectional input or output ports in any combination, or as 32 bidirectional time shared input-output ports.

Price is $2,115, 45 day delivery. For more information, contact R. A. Stevens (213) 792-1193 at 2361 E. Foothill Blvd., Pasadena 91107.



HANDY DANDY PAPER TAPE WINDER

The Handy Dandy is a hand held paper tape winder provided by SCCS member Bill Roch. Powered by four D batteries, this tape winder facilitates repeated winding of punched paper tapes into a neat roll at minimal cost — $16 shipped, and $15 if purchased at the Los Angeles general meeting of the Southern California Computer Society . . . all plus 6% sales tax. Contact Bill to place your order, or for more information at (213) 348-4278, or write 5658 Keokuk Ave., Woodland Hills 91364.



NEW DATA ENTRY DISPLAY TERMINAL

(See picture bottom of page 28)

A compact, light-weight CRT Computer Terminal has been introduced by INFORMER, INC., which permits any secretary to communicate directly with a computer. The entire desk top unit weighs ten pounds and can easily be moved. The Data Entry INFORMER works directly with a mini-computer or may be plugged into telephone lines for remote entry-even dial-up.

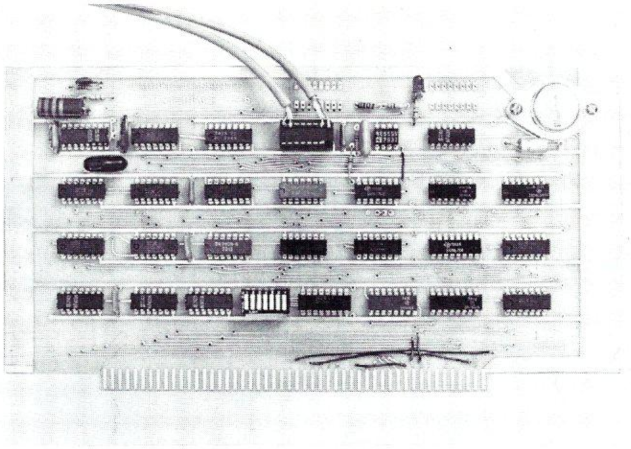
Features are standard keyboard spacing and configuration, separate 10 key number pad and special function, rotational CRT display screen, and lockability.

Total power consumption is 40 watts, and is compatible with EIA standards. List price for a single unit is $1890 in stock. For more information on the D-301 INFORMER terminal, contact Will Little or Don Sherwyn at (213) 477-4216, 2218 Cotner Ave., Los Angeles 90064.

EXECUTIVE INFORMER

Informer, Inc. is pleased to offer its Executive INFORMER CRT Display Terminal. (MODEL I-301 EXECUTIVE INQUIRY TERMINAL) This solid walnut, twenty-pound miniature device, which occupies less space on a desk than a sheet of paper, is designed to fit into any executive suite. Brochures which contain complete mechanical dimensions and electrical specifications for this RS-232 compatible unit priced at $1,850 1-4 units and $1,060 in quantities of 100, is available from Informer, Inc., 2218 Cotner Ave., Los Angeles, California 90064.

For additional information, contact Will Little or Don Sherwyn at (213) 477-4216, or circle number xx on Reader Service Card.



Don Tarbell announces the Tarbell Cassette Interface, compatible with the proposed cassette interface standards endorsed at the recent meeting in Kansas City. Features: speed up to 540 bytes per second, at 2200 bits per inch and 187 bytes per second at 800 bits per inch, phase encoded, self clocking, Altair compatible, dip switch device-code, 4 output control lines and 4 input status lines.

The Tarbell Cassette Interface is available assembled for $150, or in kit form for $100 and comes with complete assembly, maintenance and operating instructions as well as a complete set of subroutines and demonstration programs.

For more information, contact: Don Tarbell, 144 Miraleste Dr., #106, Miraleste, Calif. 90732. Phone (213) 832-0182.

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Bits & Bytes

by Mike Teener

This is not exactly the best time of year for new product announcements, but there are a few things that may interest you.

INTEL is producing, in sample quantities, their new 16K bit RAM. Full production will come within a year. Others are not far behind. This means that the price of the now standard 4K chip will be dropping even farther. But the main thing that will create an impact on our common hobby is the increase in the amount of memory we can put on one Altair-standard board. . .up to 16K bytes.

MOTOROLA now has a version of PL/M (Intel's higher level language for the 8080). They call it MPL, a really original name! Unfortunately, it also is written in FORTRAN, so we still only have basic for our machines. There is a FORTRAN available for the 8080. But it's actually more crude than either Sphere basic or MITS basic.

MITS slipped on their delivery of my Altair 680 kit, so I can't say much about it from personal experience.

The WAVE-MATE people who advertise in these pages make allusions to an upcoming APL for their system. Looks like I may have to take someone to dinner.

Since I'm always relaying to you readers some of the glut of new product announcements, it might be nice for you to know a few of the rules of this game. First, many dates mentioned are sometimes wishful thinking — witness the experience of the MITS DOS (Disk Operating System), promised first in September, 1975, then November, 1975, then December 1975. (Granted, Murphy's Law haunts most electronics manufacturers.) Second, the wording often appears to imply features or advantages that do not really exist. This is a great way to do market research. If the company making the

(Continued on page 42)

AN
INTRODUCTION
TO
MICROCOMPUTERS

From the authors of
"THE VALUE OF POWER"

Here is a book that is easy to read. It takes you by the hand, from elementary logic and simple binary arithmetic, through the concepts which are shared by all microcomputers. It tells you how to take an idea that may need a microcomputer, and create a product that uses one.

This book is complete — every aspect of microcomputers is covered: the logic devices that constitute a microcomputer system; communicating with external logic via interrupts, direct memory access and serial or parallel I/O; microprogramming and macroprogramming; assemblers and assembler directives; linking and relocation — everything you need to know if you are going to select or use a microcomputer.

These microcomputers are described in detail: The Intel 8080, the Rockwell PPS-8, the Fairchild F8, the National Semiconductor PACE and SC/MP, the Motorola M6800 and the Signetics 2650.

Copies of the book are available for $7.50, plus sales tax where applicable. Discounts are available on orders for 100 books or more.

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HARDWARE REPORT

by S. Wilcox

HARDWARE vs. POWER

This writer had encountered a problem with his ALTAIR 8800 power supply. Many ALTAIR owners, the author included, have been under the impression that the basic logic supply had a rating of 8v at 8 usable amps. For most practical purposes this is not true. With nine cards plugged into the system, 8 volts at a bus current of 6 amps was measured. It was of concern that, even though some non-MITS boards were being used, the system had run out of power when barely filled to one half physical capacity. The concern was greater when looking at the +5 volt busses after the on-card regulators. Every voltage regulator was dropping out of regulation to some extent. Some showed dropouts of 160mV.

The problem is that the +5 volt on-board regulators need a minimum voltage offset between their input and output. There is a tolerance factor, with some units ceasing to regulate when their input voltage falls below 8 volts. Then the output simply follows the input and of course any noise is guaranteed to be passed along to the on-board circuits. Some units I have seen will regulate down to within 2 volts of the output voltage. However, good engineering practice is to design for worse case conditions.

The basic principle of the capacitor filter is charge replacement. For it to be effective in preventing the ultimate ripple voltage from dipping below a minimum value, the discharge time constant of the filter capacitor and load resistance must be greater than the charging time constant formed by the filter capacitor and the output resistance of the power supply.

During the time that the power supply diodes are reverse biased, the filter must supply the entire load current.

$$I_{load} = Q_C \div \text{time}$$

This lost capacitor charge Q_C must be replaced by the transformer-rectifier during the charging time which is related to the maximum allowable ripple and the conduction angle.

$$(V_{max} - V_{ripple}(= V_{max} \sin 0$$

If the peak-peak ripple voltage were 7.2V-8.4V then $V_{ripple} = 1.2V$ and the conduction angle is approximately:

$$0 = \text{arc sin } (7.2V/8.4V)$$

$$0 = 59^\circ$$

The conduction time T_C is:

$$60\text{Hz}(T_C) = (90^\circ - 0)/360^\circ$$

$$T_C = 1.4\text{ms}$$

The charge that the transformer-rectifier must replace into the filter capacitors is approximately:

$$Q_C = CV_{max}(1-e^{t/RC})$$

As the load current is allowed to increase and therefore the charge taken from the filter capacitors, compensation can be made in several ways. The first reaction is to install larger capacitors. This is OK up to the point that the rectifiers can still handle the peak currents. For the above example with 6 amps of load current and a conduction time of approx. 1.4ms:

$$I_{peak} = (Q_C/T_C) + I_{load}$$

$$I_{peak} = 30 \text{ amps}$$

Another alternative would be a transformer with a lower output impedance. The current ALTAIR power transformer is impedance limited to the extent that at 6 amps the peak voltage is reduced by 1.6V.

$$V_p = 1.414\ V_{rms} - I_o Z_o$$

The lower output impedance would result in a faster charge replacement time constant. The last solution, which is the one chosen by MITS, is to increase the maximum charging voltage by using a higher voltage transformer. The only problem with this is that the on board regulator power dissipation goes up in direct response the increase in bus voltage.

The way the whole situation shapes up now is that the basic power supply can provide about 5 amps before the ripple valleys start to cause the regulators to drop out. A few thousand mfd. can be added to the filters to increase the available output (the author's version can push 6amps with an extra 7000mfd). Or the basic design can be beefed up with a new transformer from MITS. Personally, I feel the best solution would be to put in a higher capacity transformer, a higher current rectifier, and larger filter capacitors.

MITS says that if you have purchased at least six of their boards they will provide you with a higher voltage transformer at no cost. However they caution not to use this transformer modification with less than four cards installed in your machine.

EDITOR'S NOTE: Some of the power supply design considerations presented are approximations or "rules of thumb." For a more complete treatment the reader is referred to the following works: Ryder, J.D., ELECTRONIC FUNDAMENTALS AND APPLICATIONS; Millman & Halkias, ELECTRONIC DEVICES & CIRCUITS; Mattson, R.H., ELECTRONICS; DeFrance, J.J., GENERAL ELECTRONICS CIRCUIT.

HARDWARE FEEDBACK

Back in the December issue we reviewed the ALTAIR compatible 4k memory board designed and offered in kit form from Godbout Electronics. Although we were impressed that this was a quality piece of electronics, it did seem that it drew an appreciable amount of current, 1.7a. Most computer hobbyists, being economy minded, want only the most memory for the best price; and since most static memory boards now being offered have published current specs in the 800 ma to 1.2a range, the 1.7a didn't seem wildly outrageous. Incidently, the memory board runs beautifully at zero wait states.

Well, shortly after the December issue was released Bill Godbout called to tell us that something was definitely wrong with that particular memory board. It was only the second one out of about 1000 in use that had this excess current symptom, with the normal draw less than 1 amp. Bill was interested in having this board sent back for analysis and would even send a loan board while the other was being tested.

It is refreshing to find a manufacturer genuinely interested in his products after they are sold. The results of the analysis will come next month. In the mean time we would be interested in hearing from other members about their experiences with the Godbout unit and other 4k static memories.

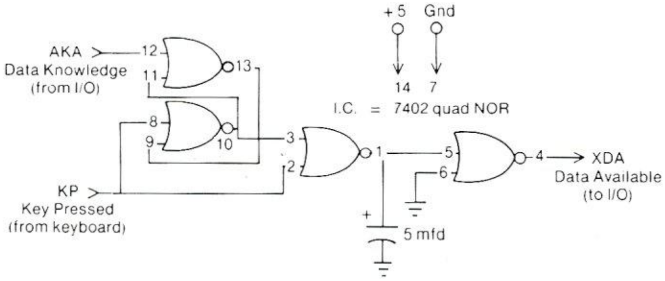
MORE HARDWARE REPORT

One of the newest entries into the ALTAIR 4k memory field is one by SOLID STATE MUSIC of Santa Clara, CA. Right now this appears to be the lowest priced 4k memory on the market at $85 thru SCCS group purchase, and in spite of the low price, the quality is high. There are sockets for all IC's and four voltage regulators on the +5 V busses for load diversity. Construction goes smoothly and should take the average kit builder 2-3 hours to complete if one can sit long enough to make the rather tedious 600 + solder joints for the IC sockets (of course the same is true of any such project). One nice feature is the elimination of the board address select jumpers which are replaced by a small convenient DIP switch. Four positions of this switch handle the memory block selection and two other switch sections control the number of WAIT states inserted per memory reference instruction. The memory chips used are a house number but equivalent to 2102's.

The author's board went together with no problems and ran perfectly the first time it was plugged in and powered up. This particular board runs at maximum CPU speed with zero wait states. Congratulations to Solid State Music on a fine kit.

HARDWARE MODIFICATION FOR KEYBOARD INTERFACE

Here is a simple circuit that was designed to interface a Southwest Technical Products ASCII keyboard to a Processor Technology 3P+S I/O port. By using the keyboard only instead of a complete TV typewriter this can be the input device for your system if you chose one of the other video display systems now on the market.



The one IC can be mounted on the keyboard printed circuit board and wired with prototype techniques.

This space contributed by the publisher as a public service.

A MESSAGE FOR DADDIES

They'd rather have you around than your insurance.

Get yourself a good, thorough examination once a year. Once a year, let your doctor really look you over. It'll take a little time, and a little patience. And maybe he'll poke around a little more than you'd really like. And so he should.

The whole idea is to keep you healthy. If nothing's wrong (and more than likely, there isn't) hooray! Come back next year. But if anything's suspicious, then you've gained the most important thing: time.

We can save 1 out of 2 persons when cancer is caught in time, caught early. That's a good thing to know. All Daddies should know how to take care of themselves so that they can have the fun of taking care of their kids. Remember—it's what you don't know that can hurt you.

American Cancer Society

APPLICATIONS EXCHANGE

by Larry Press

Last month I asked what everyone plans to do with their computers and a few people have let me know.

George Tate is into GAMES and is putting together a GAMES LIBRARY. He has facilities for handling paper or magnetic tape and would like to get copies of your game playing programs for the library. This will be a two-way street — he will also distribute game playing programs as soon as he gets the library organized. I just gave George two shoeboxes full of BASIC games . . . why don't you do the same? That's George Tate, 3544 Dahlia Ave., Los Angeles 90026.

These shoeboxes full of paper tapes which I gave to George also contained a PILOT interpreter, written in BASIC. Anyone have any interesting PILOT programs?

I have also heard from Bill Roch, 5133 Catalon Ave., Woodland Hills 91364, who has a program which converts dates to inters. Contact Bill if you're interested.

Art Childs, 335 N. Adams St., Glendale 91206 is interested in BIO-RYTHMS. Here is what Art has to say on the subject:

> "During the past few years a theory generally referred to as the 'bio-rythm' theory has become quite popular. Very simply stated, the proponents of bio-rythm contend that the three major aspects of the human being, i.e.: mental, physical and emotional abilities, are cyclical in nature and that the timing of these cycles is predictable for all humans.
>
> "This theory has found acceptance by some major corporations throughout the world. Some of these corporations have adopted the policy of sending employees with a critical function home on those days that the bio-rythm theory predicts to be dangerous for them. For example, an engineer of a high speed train, or the pilot of a passenger airline might be sent home rather than make his scheduled run on the days that any two of his cycles cross the median line.
>
> "A more positive approach to utilizing this information about someone might be to predict (or attempt to predict) when two, or even all three, of his cycles are 'high', or right for maximum efficiency and performance.
>
> "To determine someone's cycles one simply starts with the day he was born, and calculates 23 days for his physical cycle, 28 days for his emotional cycle and 33 days for his mental or intellectual cycle."

Art suggests getting a bio-rythm package up and checking to see if correlations exist between the bio-rythmic cycles of various ball players and their performance on the field. I think that I've heard a couple of commercial outfits that run bio-rythm charts for a fee. Anyone know their addresses?

Art cautioned that his application idea was from "left field", but sent it in anyhow. Another left field application that I'd like to hear more about is BIO-FEEDBACK. The Peoples Computer Company (a newspaper) P.O. Box 310, Menlo Park 94025, announced that they will publish a Bio-Feedback section beginning with their next issue. If any SCCS people are experimenting with bio-feedback, please drop the Application Exchange a line.

8080 ADDRESS COMPARISON SUBROUTINE

Often, in the course of writing assembly language programs, it becomes necessary to compare two addresses, and build into the program certain logic based on the results of that comparison. Because the addresses are 16 bit data no one or two instructions will do the job. The following routines, however, will accomplish the task with minimum memory requirement.

In the main line (or calling routine) load the H & L with one of the addresses to be compared:

```
LHLD    ADDR1
XCHG
```

Then load H & L with the pointer to the other address, and call the subroutine:

```
LXI H,ADDR2+1
CALL ADCK
```

In the subroutine, first compare the high order. If a difference is found, the low order need not be compared, so a return is made on a minus condition:

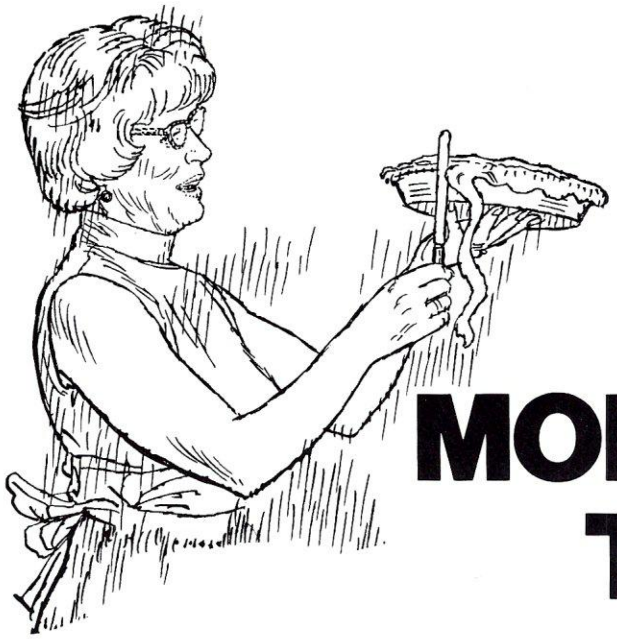
```
ADCK:   MOV A,M
        CPA D
        RC
        DCX H
        MOV A,M
        CPA E
        RET
```

If ADDR1 is equal or less than ADDR2, the carry bit will not be set, and a subsequent decision may be made on its state. Or the decision could be based on the state of the zero bit if only an equal condition were sought.

Should the logic of the program demand to know if ADDR2 were equal to or less than ADDR1, simply put ADDR2 in the D & E registers, and the ADDR1 pointer in the H & L. Or, write the subroutine as follows:

```
ADCK:   MOV A,D
        CPA M
        RC
        DCX H
        MOV A,E
        CPA M
        RET
```

The same technique may be used for comparing 16 bit values basing decisions on the carry bit rather than the sign bit.



MORE BASIC THAN BASIC

by Don Tarbell

Basic is an excellent language for the novice home computerist. The power inherent in this easy-to-use interpreter, and its availability for small computers as well as time-share systems, has in the past — and will in the future — facilitate the transformation of mere ideas into working programs, particularly for those to whom the workings of a microprocessor is a mystery. With the use of basic, most applications, whether games designed for education or simple pleasure, or problem-solving programs of a more serious nature, can be easily and rapidly programmed and enjoyed.

One area however, in which basic because of its nature, is not suitable is that of real-time applications. Eventually, many avocational programmers will encounter the problem of time, and of necessity will learn to program their microcomputer in assembly language.

The Altair Basic Interpreter, with its "Peek and Poke" capability, can be an aid to learning to handle the 8080 based microprocessor at the assembly language level. The following disassembler, contributed by Don Tarbell, when used to investigate the techniques of the professionals, will reveal many "tricks of the trade" for producing tight, efficient machine language routines.

```
LIST

9  DIM H$(16)
10  H$(0) = "0":H$(1) = "1":H$(2) = "2":H$(3) = "3"
13  H$(10) = "A":H$(11) = "B":H$(12) = "C":H$(13) = "D"
14  H$(14) = "E":H$(15) = "F"
20  H$(4) = "4":H$(5) = "5":H$(6) = "6":H$(7) = "7"
30  H$(8) = "8":H$(9) = "9"
100  INPUT "STARTING ADDRESS";S
200  INPUT "ENDING ADDRESS";E
300  FOR N = S TO E
400  X = PEEK(N)
450  B$ = H$(X/16) + H$(X AND 15)
460  A$ = H$(N/4096) + H$(N/256AND15) + H$(N/16AND15) + H$(NAND15)
500  Y = X
545  RESTORE
550  FOR I = O TO X
560  READ M$
570  NEXT I
600  IF Z  32 OR X  95 THEN Y = 32
700  IF X  159 AND X  224 THEN Y = X-128
800  PRINT A$;TAB(6);B$;TAB(10);CHR$(Y);TAB(30);M$
900  NEXT N
1000  DATA NOP,LXI B,STAX B,INX B,INR B,DCR B,MVI B,RLC
1001  DATA "  ",DAD B,LDAX B,DCX B,INR C,DCR C,MVI C,RRC
1002  DATA "  ",LXI D,STAX D,INX D,INR D,DCR D,MVI D,RAL
1003  DATA "  ",DAD D,LDAX D,DCX D,INR E,DCR E,MVI E,RAR
1004  DATA "  ",LXI H,SHLD,INC H,INR H,DCR H,MVI H,DAA
1005  DATA "  ",DAD H,LHLD,DCX H,INR L,DCR L,MVI L,CMA
1006  DATA "  ",LXI SP,STA,INX SP,INR M,DCR M,MVI M,STC
1007  DATA "  ",DAD SP,LDA,DCX SP,INR A,DCR A,MVI A,CMC
1008  DATA mov b,b","MOV B,C","MOV B,D","MOV B,E"
1009  DATA "MOV B,H","MOV B,L","MOV B,M","MOV B,A"
1010  DATA "MOV C,B","MOV C,C","MOV C,D","MOV C,E"
1011  DATA "MOV C,H","MOV C,L","MOV C,M","MOV C,A"
1012  DATA "MOV D,B","MOV D,C","MOV D,D","MOV D,E"
1013  DATA "MOV D,H","MOV D,L","MOV D,M","MOV D,A"
1014  DATA "MOV E,B","MOV E,C","MOV E,D",MOV E,E"
1015  DATA "MOV E,H","MOV E,L",MOV E,M","MOV E,A"
1016  DATA "MOV H,B","MOV H,C","MOV H,D","MOV H,E"
1017  DATA "MOV H,H",MOV H,L","MOV H,M","MOV H,A"
1018  DATA "MOV L,B","MOV L,C","MOV L,D","MOV L,E"
1019  DATA "MOV L,H","MOV L,L","MOV L,M","MOV L,A"
1020  DATA "MOV M,B","MOV M,C","MOV M,D","MOV M,E"
1021  DATA "MOV M,H","MOV M,L","HLT,"MOV M,A"
1022  DATA "MOV A,B","MOV A,C","MOV A,D",mov a,e"
1023  DATA "MOV A,H","MOV A,L","MOV A,M","MOV A,A"
1024  DATA ADD B,ADD C,ADD D,ADD E,ADD H,ADD L,ADD M,ADD A
1025  DATA ADD B,ADD C,ADD D,ADD E,ADD H,ADD L,ADD M,ADD A
1026  DATA SUB B,SUB C,SUB D,SUB E,SUB H,SUB L,SUB,M SUB A
1027  DATA SBB B,SBB C,SBB D,SBB E,SBB H,SBB L,SBB M,SBB A
1028  DATA ANA B,ANA C,ANA D,ANA E,ANA H,ANA L,ANA M,ANA A
1029  DATA XRA B,XRA C,XRA D,XRA E,XRA H,XRA L,XRA M,XRA A
1030  DATA ORA B,ORA C,ORA D,ORA E,ORA H,ORA L,ORA M,ORA A
1031  DATA CMP B,CMP C,CMP D,CMP E,CMP H,CMP L,CMP M,CMP A
1032  DATA RNZ,POP B,JNZ,JMP,CNZ,PUSH B,ADI,RST 0
1033  DATA RZ,RET,JZ "  ",CZ,CALL,ACI,RST 1
1034  DATA RNC,POP D,JNC,OUT,CNC,PUSH D,SUI,RST 2
1035  DATA RC,"  ",JC,IN,CC,"  ",SBI,RST 3
1036  DATA RPO,POP H,JPO,XTHL,CPO,PUSH H,ANI,RST 4
1037  DATA RPE,PCHL,JPE,XCHB,CPE,"  ",XRI,RST 5
1038  DATA RP,POP PSW,JP,DI,CP,PUSH PSW,ORI,RST 6
1039  DATA RM,SPHL,JM,EI,CM,"  ",CPI,RST 7

OK
```

Letters to the Editor

Dear Editor:

The December issue of INTERFACE invites other clubs to send news so I'd like to tell your readers a little about LO*OP Center. The Center is a non-profit educational resource facility and we happen to think computers are about as powerful a resource as learners are going to find outside their own brains. We operate a storefront computer center where anyone can walk in, play games, study programming or buy terminal time. In addition we are trying to fill the gap between the computer freak — be (s)he hobbyist or vendor's representative — and us ordinary folk — teachers, students, consumers, apprehensive curiosity seekers. We do this with "Meet the Computer Classes" for children and adults, offering consulting services to schools and other organizations who want to get into computers, and publishing wherever and whenever we can.

Any of your readers who are interested in education can help us. We need contributions of games which teach something — anything except hunt and kill. We have a D.E.C. Classic (PDP8/a with floppies) running under OS/8 and a PDP8/1 running Edusystem 20 version c. Our Altair 8800 still has 256 words but we can start collecting software now. Everything reads paper tape.

We need staff — teachers, hardware and software people, and stamp lickers. And of course, we need money. Memberships run from $24 to $500 per year. We'll send literature to anyone who requests it, or come for a visit next time you're near San Francisco (Cotati is 40 miles north on Rte 101). Many thanks,

Liza Loop, director
LO*OP Center

Ed.

*It is gratifying to know there are organizations in the country like LO*OP Center who's goal is to get computers and computer power to the people.*

Dear Editor:

I understand and appreciate the desire to change the publishing of INTERFACE. The original newsletters seemed more personal — (you to me). The new copy has great prints and diagrams — but I would like to see the articles continue on consecutive paper as much as possible.

I'm absolutely sure I'm going to get as much or more from each of the following issues as I have in the past.

Manley Nichols

Ed.

Thanks for your comments. We appreciate the feedback.

Dear Mr. Childs:

This morning I received my December issue of INTERFACE.

I assume that MITS contributed heavily to the cost of producing this issue of INTERFACE, and I do not object to your accepting their nine pages of advertising (page 16 and the un-numbered pages following). I don't think that the SCCS should be officially touting the two MITS computers as "The People Computers" in full color on the front page of their only official publication. I, too, feel that small computers are becoming "people computers", as they become more available and easier to use. But there are several companies manufacturing small computers and small computer components. At worst you should have included two or three other different kinds.

Now that that's off my chest, I can sit down and enjoy those pages of INTERFACE which you sent.

Kenneth Yapkowitz
1321 Keniston Ave.
Los Angeles, California 90019

Ed.

Thanks for your response to our first (December, 1975) magazine issue, Ken. I trust succeeding issues of INTERFACE have helped clarify the fact that the only thing we officially tout is home computing.

Dear Interface:

ON STANDARDS. What this hobby field needs are some good standards to facilitate meaningful interchange between users. Standards can either evolve from the various manufacturer's systems with the most popular becoming the defacto standard (shades of IBM) or system standards can be dictated from the onset by committee and/or manufacturer's mutual agreement as was recently done at the Kansas City conference on hobbyist digital tape recording techniques.

Popular Electronics with it's recently added "Computer Bits" column will, I am sure, do much to foster and influence both software and hardware standards for the computer hobby. The mere fact that

PE does publish something almost guarantees that it will be a "popular" standard and also, of necessity, a generalized standard. We also need detailed specific standards now in several areas in which SCCS could be instrumental in forming the standards guidelines.

What do you do if you want to plug in your parallel 8 bit I/O terminal into someone else's ALTAIR? There seems to be no firm hardware standards for input/output connections. And unless two users have agreed on their interconnect scheme, they are in trouble. The problem is that you wire your system connectors one way and someone else uses another method. MITS suggests one type "standard" pin allocation for the 25 pin Dataphone D type backpanel connectors. This would be fine if we all agree to abide by it. But wait a minute, what about the new IMSAI System owner who knows nothing of the MITS "standards" and both systems are functionally fully compatible. Perhaps if there were more IMSAI systems in the field there would be a move to standardize on their interconnection scheme. For a TTY interface there is the same problem of direct plug compatibility. However, I understand that EIA does have a standard for RS232 D type connectors. Perhaps someone could comment further on this.

Getting the right data and handshake lines to the right connector pins is only half of the problem. How should we standardize the signals on these pins? I don't mean signal levels; we all know of TTL, current loops, and EIA signals. The question is whether data true active is going to be low or high. For TTL levels all signals **should** be true active low since a disconnect or other open circuit in a system using active high signals is sensed as true. In practice the data lines usually are true high and the control lines a mixture of true high and true low signals. WE NEED A STANDARD.

There are already on the market several non-compatible I/O interfaces with more to come. I would appreciate further member comments on the problems of standards, and the possible formation of an SCCS Standards committee. These are the formative months for our hobby; the time for action is NOW.

S. Wilcox
Alhambra, Calif.

Ed.

We agree. INTERFACE will support a hardware standardization effort to the fullest. Interested individuals like yourself are invited to comment and/or volunteer to serve on a hardware standards committee.

Dear Editor:

Congratulations on a splendid inaugural issue of INTERFACE! Great cover!

True Seaborn
Editor and Publisher
Computer Magazine
(IEEE Computer Society)

Ed.

Thank you.

Dear Editor:

Would seem to me that at least the spirit of your free, non-commercial guide in the front cover has been violated by at least one of the ads in this your 1st issue — i.e., what are the member names & addresses of the two center column ads. Those of us wishing to publish want ads for personnel to run a money-making business should pay the inexpensive commercial ad rate!?

Your 55c postage is 4 times the amount I see on much heavier material; that's two thirds of the annual dues!

J. Brown
Anaheim, California

Ed.

In the hopes of possible member benefit, the two ads to which you refer were run before SCCS policy regarding employment ads had been established. The EMPLOYMENT QUEUE and the attendant policy will now allow us to serve the membership in that area and maintain the integrity of the free member ad policy.

Regards the postage — we hope to have our second class permit soon. In the meantime we will be exploring alternatives with our commitment to the members foremost in mind.

To The Readership

Our purpose is to support the home computerist. To accomplish this we want to reach as far and wide as the Postal Service will allow. It makes no difference if you grow potatoes in Idaho, manufacture cars in Detroit, chase cows and oil wells in Texas, or simply enjoy retirement in Florida. You are invited to become a member of SCCS, a reader of INTERFACE and a member of that rapidly growing community of people who are discovering IBM has no monopoly on computers!

From The Editor

SCCS MEMBERSHIP NUMBER

Do you need to know your membership number? Perhaps you did know, but forgot it. You can find it — and be reminded each month — by looking on the SCCS INTERFACE mailing label.

Group Purchase For SCCS Members

A group purchase program has been established to enable all SCCS members to participate in the buying of selected products at discounted rates. To find out products and prices, a taped telephone message is prepared monthly, (213) 438-3890, with updated information. The tape states the date of the recording so callers can verify that they have current data. Announcements of available products will be made at each SCCS monthly meeting, and the tape is then updated. But please allow three days after the meeting for preparation of the new message before calling.

Since the message is stated only once and very quickly, it is suggested that a cassette recorder be used to make a permanent record of the information. The message will mention the product name and price only. For complete details on products listed, refer directly to the manufacturer or product vendor.

ORDER DEADLINE IS THE FIRST OF EVERY MONTH. Orders received on the first of the month prior to meeting date will be delivered at the meeting. Group purchase is based upon quantity requirement — if the minimum is not met, either a refund of your money, or holdover of delivery until the following month, may be required. Those who wish to receive shipment by UPS must add 5% to their purchase price to cover shipping and insurance. A 1% add-on (or $1, whichever is greater) is required to cover handling costs. California residents must add 6% sales tax to the total purchase price.

Send your check or money order, made out to the Southern California Computer Society Trust A, along with the order form, below.

GROUP PURCHASE ORDER FORM

Clip and mail this order form, with your check or money order, to

SOUTHERN CALIFORNIA COMPUTER SOCIETY
P. O. Box 987
South Pasadena, California 91030

Member Name ______________________
Membership # ______________________
Address ______________________
Street City State Zip

I will pick up my order at the next SCCS meeting ☐

Please ship my order to me, for which I have included 5% for shipping and insurance. ☐

QUANTITY	ITEM/DESCRIPTION	UNIT PRICE	TOTAL

Sub Total	
1% Handling ($1 minimum)	
6% Sales Tax	
5% Shipping and insurance	
TOTAL ENCLOSED	

by Ralph Klestadt

Graphics and plotting in large systems is one of the important, yet not often explored, aspects of large scale systems. Financial graphics, scientific and mathematical plotting, as well as Computer Aided Design (CAD) are quite interesting and deserve some further exploration.

Although there are not many routines for financial plotting and graphing, it is not difficult. For example, plotting the curve of the stock market with it's daily highs and lows can be done by using first a routine to plot the basic average curve of the market, with all the points recorded in the program. Then, you might use another routine that only plots straight lines to project out so many points from each coordinate on the curve. Large scale systems are probably the best for plots like these as they can keep track of, and utilize, more data than a minicomputer can.

Trend analysis and plotting of linear regression can be done quite easily utilizing some of the features of the higher level FORTRANS, such as FORTRAN G and FORTRAN-10. Usually the routines to be used are dictated by the contents of the installation library. Mathematical plots are more often easily done, although the experience I have had with FORTRAN in this application has not been very favorable. Almost every installation has its own set of stock mathematical plotting routines, which may be used in any combination through a main calling program to give suitable plot. For example, you may use routines to plot perpendicular axis for a graph, use a routine for plotting parabolas, and finally use a routine to give a title and document the graph.

In Computer Aided Design, mechanical details and integrated circuit diagrams have to be actually drafted out by the computer. I cannot go into much of an explanation here, as this field is perhaps the most highly specialized field of plotting and each installation has its own routines specifically tailored to its own specifications. The designer will often set a list of rules for the routine to follow and then the routine will scan these rules to plot the circuit.

Plotting routines on batch machines can vary greatly, from routines that will take defaults on your plots, rendering them easy to use, to those that practically demand a particular make of plotter. Plotting on IBM batch systems is usually handled through many FORTRAN routines, as well as some straight system routines. Most plotting routines on systems like these are quite extensive and making a simple plot of a curve can often be quite difficult. On the other hand, 5 color, 3-D plots of the globe on a polar angle appear to be quite easy!

This apparent contradiction can be exemplified at the University of Southern California. As far as I have found, USC does not have a routine to plot a straight line alone. Straight lines can be plotted as long as they are with other lines of other curves. Yet, in the display room there are plots of the globe from a polar view plotted in five colors. As I recall, it says, "In order to get a plot of this, simply say: 'CALL GLOBE'." Incidentally, that plot has no straight lines.

The manufacturer of the plotter will usually offer routines for plotting bar graphs and curves. Normally, the company supplied plotter routines are easier to use than installation supplied routines or IBM supplied routines. The Control Data 3150 (as used at California State University, Northridge) is only accessible through their FORTRAN. Although these routines are not as extensive as some other plotting routines, they are very easy to use and are flexible to an extent.

TOWARD THE UNDERSTANDING OF LARGE SCALE SYSTEMS

(Part III)

Perhaps the most interesting part of large scale system graphics is on the timesharing and real-time systems. Most graphics work on timesharing systems is done on the CRT terminal, as it does not waste plotter paper testing plots, and it doubles as the computer terminal. CRT terminals with built in hard copy capability are particularly nice for on-line graphics work since a plot can be quickly duplicated on paper when needed. Plotting capability on the CSUN Control Data System is virtually nonexistent on the FORTRAN there. DEC offers a rather large plotting library that affords fine interaction between their monitor, the user terminal, and the plotting routines.

The plotting program with your data can be run interactively under the timesharing monitor, write the plot onto disk after you've checked it out, or print and copy it on your CRT. When on disk, it can be plotted wherever and whenever convenient. Yet, this plotting is not limited to user-interactive work. A large aerospace firm uses a DECsystem-10 for CAD (Computer Aided Design). This work entails items such as integrated circuit design, which almost necessitates a computer doing the drafting. This is due to the intricacy of the work which does not allow for human error. An error here may cost a company millions of dollars in the future. Much work on plotting deals with the capabilities of the language of the plotting programs, which in turn depend greatly on the machine. Usually it is FORTRAN that does the duty here. In general, a plotting/graphics routine on large scale timesharing systems will be contained in the terminal being used at the time.

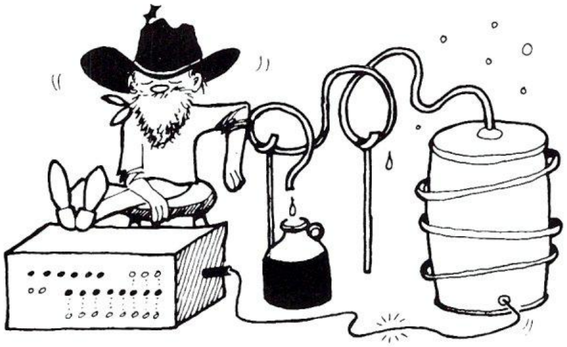
As graphics becomes more prominent, we should be seeing major developments in software and some in hardware. Currently, however, the available hardware will accomodate graphics routines. Although many aspects of this field still remain specialized, there are a few general plotting systems appearing on the market.

A number of new systems are being designed around the intelligent remote terminal concept. Under this philosophy, the remote terminal being used has graphics capability and can do some graphing on its own (it is generally a CRT), and uses minimum central processor time. The DEC VT40 terminal is a good example of this. It is a CRT terminal driven by a PDP-11/10 minicomputer. It can run some pretty fancy plots alone, yet does not have the capacity to hold as much data or do computations necessary for the plot as rapidly as most large scale systems.

At USC, they are using a PDP-11/45 in their laser-research laboratory connected to a Tektronics CRT terminal. The 11 has its own operating system, yet most of the work is done through the 11 to the main DECsystem-10 which serves the entire engineering complex. Examples like this show us how the large scale processor can be utilized most efficiently. If straight computation is accomplished on the big system the plots and other output go through a remote system, whether its intelligent terminal or end-minicomputer, to be plotted or printed. Unfortunately I do not have much experience in this aspect of graphics, since I'm limited to hardcopy terminal, which, although may be used for abstract plots, is not recommended for accurate and demanding plots.

Graphics capability on large scale systems seems to be a somewhat neglected area. Perhaps with the appearance of less expensive CRT terminals, more powerful and easier to use graphics software will be developed and made available to the small user. ◻

GAMES & THINGS



SLOT MACHINE GAME For MITS BASIC

by Jon Walden

This program is written using the combinations and percentages suggested by Donald D. Spencer on pages 219-223 of his book, "Game Playing with Computers".

SLOT MACHINE IS SET UP WITH 3 REELS, 20 SYMBOLS EACH REEL:

	REEL 1	REEL 2	REEL 3	SYMBOL	EQUIVALENT
CHERRIES	4	6	0	=	1
ORANGES	5	4	7	0	2
BELLS	4	6	5	1	3
LEMONS	3	2	4	#	4
WATERMELONS	3	1	3	+	5
BARS	1	1	1	$	6

PAYOFFS ARE AS FOLLOWS: (A = ANY SYMBOL)

COMBINATION			PAYOFF	NUMBER OF POSSIBLE WAYS
=	A	A	$ 3	400
=	=	A	5	240
0	0	$	6	20
1	1	0	8	168
#	#	#	10	24
+	+	$	15	3
0	0	0	18	140
+	+	+	20	9
$	$	$	200	1

PAYOFF AVERAGES $70.49 FOR EVERY $80 PUT IN; NET LOSS IS $9.51; THE HOUSE MAKES 11.89%. (CASINOS ARE THOUGHT TO MAKE BETWEEN 3% AND 50% WITH THE AVERAGE BETWEEN 11% and 12%.)

EACH TIME THE REELS SPIN YOU ARE BETTING A DOLLAR. THE PROGRAM ESTABLISHES THE REEL EQUIVALENTS WITH RANDOM NUMBERS, PRINTS OUT THE SYMBOLS, THE PAYOFF (IF ANY), AND SUMMARIZES YOUR FINANCIAL POSITION AT THAT POINT. (REMEMBER IF YOUR WINNINGS ARE $20 AND YOU WIN A $5 PAYOFF, YOUR NEW WINNINGS ARE $24 — $25 MINUS THE DOLLAR YOU BET.)

THE PROGRAM IS WRITTEN IN 'MITS' BASIC AND USES THE FOLLOWING VARIABLES:

K	PAYOFF COUNT
L	LOSSES (MONEY PUT IN)
N	NUMBER OF RANDOMS IGNORED
P	PAYOFF
Q	EQUIVALENT OF ALL THREE REELS
R(3)	EQUIVALENT OF INDIVIDUAL REELS
S(6)	SYMBOL EQUIVALENT TABLE
W	WINNINGS (TOTAL PAYOFFS)
X/Y	'FOR' LOOP CONTROLLED VARIABLES
Z	IGNORED RANDOMS

D$	DECISION
R$(3)	SYMBOL FOR INDIVIDUAL REELS
S$(6)	SYMBOL TABLE

I'd like to say something brief about MITS Basic: I think it's great! Comments have been made about it being slow and about certain clumsy features. But the agility to play with bits, to sense ports and to use single ASCII codes is long overdue! I hope the use of "INP" in this program will encourage other programmers to work on new data input methods (especially for games). Having to "hit return" after each entry is a drag!

```
100  DATA = ,0,1,#, + ,$
110  FOR X = 1 TO 6:READ S$(x):S(X) = X:NEXT
120  IF NOT (INP(0)<128) G010 120
130  OUT 1,12
140  PRINT 1AB(6);">>>>>> SLOT MACHINE<<<<<<":PRINT:PRINT
150  N = INT (500*RND (8)) + 1
160  FOR X = 1 10 N:Z = RND(8): NEXT
170  PRINT "PRESS THE SPACE BAR TO GET REPEATED"
180  PRINT "REEL SPINS. (EACH SPIN COSTS YOU $1.)"
190  PRINT:PRINT "PRESS 'Q' WHEN YOU'RE READY TO QUIT."
200  PRINT:PRINT "PRESS ANY OTHER KEY TO GIVE YOURSELF"
210  PRINT "A BREAK. THE SPACE BAR WILL GET YOU"
220  PRING "GOING AGAIN . . . GOOD LUCK!!!"
230  IF NOT (INP(1) = 32 OR INP (1) = 81) GOTO 230
240  IF INP (1) = 81 GOTO 750
250  L = L + 1
260  FOR X = 1 TO 3:R(X) = INT(20*RND(8)) + 1:NEXT
270  IF R(1) < 6 THEN R(1) = 2:GOTO 330
280  IF R(1)<10 THEN R(1) = 1:GOTO 330
290  IF R(1)<14 THEN R(1) = 3:GOTO 330
300  IF R(1)<17 THEN R(1) = 4:GOTO 330
310  IF R(1)<20 THEN R(1) = 5:GOTO 330
320  R(1) = 6
330  IF R(2)    7 THEN R(2) = 3:GOTO 390
340  IF R(2)  13 THEN R(2) = 1:GOTO 390
350  IF R (2)  17 THEN R(2) = 2:GOTO 390
360  IF R (2)  19 THEN R(2) = 4:GOTO 390
370  IF R(2) = 19 THEN R(2) = 5:GOTO 390
380  R(2) = 6
390  IF R(3) < 8 THEN R(3) = 2:GOTO 440
400  IF R(3)<13 THEN R(3) = 3:GOTO 440
410  IF R(3)<17 THEN R(3) = 4:GOTO 440
420  IF R(3)<19 THEN R(3) = 5:GOTO 440
430  R(3) = 6
440  Q = 100*R(1) + 10*R(2) + R(3)
450  IF Q = 666 THEN P = 200:GOTO 550
460  IF Q = 555 THEN P =   20:GOTO 550
470  IF Q = 222 THEN P =   18:GOTO 550
480  IF Q = 556 THEN P =   15:GOTO 550
490  IF Q = 444 THEN P =   10:GOTO 550
500  IF Q = 332 THEN P =    8:GOTO 550
510  IF Q = 226 THEN P =    6:GOTO 550
520  IF INT (Q/10) = 11 THEN P = 5:GOTO 550
530  IF INT (Q/100) = 1 THEN P = 3:GOTO 550
540  P = 0
550  FOR X = 1 TO 3:FOR Y = 1 TO 6
560  IF R (X) = S(Y) GOTO 580
570  NEXT Y
580  R$(X) = S$(Y):NEXT X
590  W = W + P:IF P = 0 GOTO 610
600  K = K + 1
610  PRINT:PRINT "REELS:"TAB(9);R$(1);TAB(12);R$(2);TAB(15);R$(3)
620  IF P = 0 GOTO 700
630  IF P = 200 GOTO 660
640  IF NOT (INP(0)<128) GOTO 640
650  OUT 1,7:PRINT "PAYOFF: $";P:GOTO 700
660  FOR X = 1 TO 75
670  IF NOT (INP(0)<128) GOTO 670
680  OUT 1,7:NEXT
690  PRINT "JACKPOT!!!!!! $";P
700  ON SGN(W-L) + 2 GOTO 710,720,730
710  PRINT "SO FAR YOU'VE LOST $";L-W:GOTO 740
720  PRINT "SO FAR YOU'RE EVEN":GOTO 740
730  PRINT "SO FAR YOU'VE WON $";W-L
740  PRINT:GOTO 230
750  PRINT:PRINT "TIMES PLAYED: ";L:PRINT "NUMBER OF PAYOFFS: ";K
760  PRINT "AMOUNT PAID: $";W
770  ON SGN (W-L) + 2 GOTO 780,790,810
780  PRINT "TOTAL LOST: $";L-W:PRINT "WANNA TRY AGAIN, SUCKER?":GOTO 9999
790  PTINY "YOU BROKE EVEN. TOO BAD,":PRINT "THE NEXT ONE MIGHT HAVE"
800  PRINT "BEEN THE BIG ONE!":GOTO 9999
810  PRINT "TOTAL WON: $";W-L:PRINT "YOU BUY THE DRINKS!"
9999  END
OK
```

(*Continued from page 17*)

These languages use mathematical and English notation. The following is an example of a programme written in BASIC:

```
10  INPUT A
20  IF A <0 THEN 50
30  GO TO 10
50  END
```

Here, no "intimate" knowledge of the functioning of the computer is required; it is sufficient simply to know the syntax and the semantics of the particular language used.

In the same way that a symbolic programme is translated into binary by an assembler programme, a programme written in an evolved language must be translated into executable machine language form by a special programme called the *"compiler"*, the process being called *"compilation"*.

Thus, both assembler and compiler have the same function; however, the compilation of an instruction written in an evolved language may give rise to several binary instructions.

BITS & BYTES

(Continued from page 30)

announcement gets many inquiries regarding the implied feature, it may actually provide them. Third, don't get mad when the first two items turn out to be true; this industry is incredibly competitive — which is to our advantage in the long run.

LEASE A TELETYPE

Do you want a teletype but can't afford the $900 or so for a reconditioned ASR33? Try leasing one. American Used Computer (Box 68, Kenmore Station, Boston, Mass. 02215) will give you one for $35 a month on a two year lease, or $30 a month for three years. There are lots of other companies doing terminal rental/leasing/ sales. Look around and you may find even better deals.

"A LEADER IS . . ."

Significant differences between a Boss and a Leader could be explained as follows:

"A Boss creates fear — A Leader creates confidence.

Bossism creates resentment — Leadership breeds enthusiasm.

A Boss says 'I' — A Leader says 'We.'

A Boss fixes blame — A Leader fixes mistakes.

A Boss knows how — A Leader shows how.

Bossism makes work drudgery — Leadership makes work interesting.

A Boss relies on authority — A leader relies on cooperation.

A Boss drives — A Leader leads."

Second part
Application to microprocessors

Chapter I
MICROPROCESSORS

Before applying what has been said in Part I to the MOTOROLA MPU, it seems useful to give a few characteristics of microprocessors in general, their advantages and disadvantages, their applications and selection criteria.

1. General

Microprocessors are often referred to as "MOS/LSI computers on a chip". This rather dangerous label calls for a word of warning: the microprocessor and the associated components needed for its operation must certainly not be regarded as the "miracle product" capable of equalling or surpassing the performance of a computer; the microprocessor is quite incapable of doing so, at least for the time being. On the other hand, it is correct to say that in most cases the microprocessor can advantageously replace a wired logic system of some importance.

It is therefore essential to stress from the start that the characteristics of the microprocessor are not to be considered relative to the performance of a computer or even a mini-computer but rather should be compared with the characteristics of a wired logic system.

2. Advantages

2.1. *Flexibility*

The main advantage of the microprocessor is certainly its flexibility, that is, its capability of improving and extending the possibilities of a basic system. This optimization of the initial possibilities of a system is obtained essentially by means of software and not by major changes in the hardware circuits of the system.

2.2. *Cost of the system* (see § 3.2.)

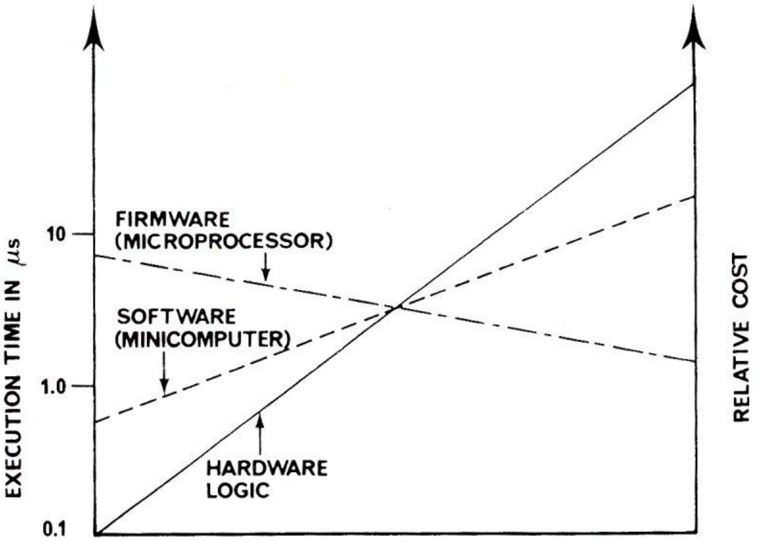
3. Disadvantages

3.1. *Software*

Utilization implies that, the designer familiarizes himself with a discipline which he does not necessarily know much about or which he only rarely has occasion to use, viz., programming.

3.2. *Speed*

A microprocessor using MOS technology is slower than an ECL wired logic system for example.
Despite the advent of MSI and LSI circuits which are also capable of performing complex functions, the incorporation of these circuits in a large digital system is still too difficult and costly for them to be preferred to microprocessors.
The chart below gives an idea of the cost of microprocessor and wired logic systems as a function of execution times of the functions performed by the systems.



4. A few possible applications

The principle of the microprocessor is to perform the functions programmed in its Read Only Memory; this fixed programme which can not be modified is termed *firmware.*
This principle differs, on the one hand, from that of general purpose computers programmed by software and, on the other hand, from that of digital systems which can only perform the function which was wired into them.
Different programmes may be stored in the ROM of the microprocessor system to cover the following applications:
- point of sale terminal
- inventory control
- telecommunications control
- chemical analysis

- control of machine tools
- multiprocessor minicomputer
- bank terminal
- intelligent terminal
- medical electronics
- optical character recognition, etc.

5. Design considerations

It is necessary to make a preliminary evaluation of the requirements of the system to be designed before making a definitive choice in favour of wired logic or the microprocessor. The requirements to be taken into consideration include the following:

5.1. *Functions to be accomplished*

The number and type of functions to be performed determine the basic architecture of the system. The use of a microprocessor is possible or even essential when the system involves arithmetic, control and decision functions and above all when it must keep track of the operations which it has already carried out in order to be able to perform the operations which follow. As a general rule, any system where the operation resembles that of a computer may use a microprocessor as a basic building block. Computer architecture allows the repetitive and continuous use of the hardware to achieve a maximum of functional operations.

5.2. *Size of hardware required*

The hardware requirements determine the physical size of the system. This size may be estimated by answering the following questions:

- How many channels are necessary to acquire and transmit the information?
- Do these channels operate at the same speed? Do they exchange serial or parallel information? Do they operate according to a given sequence?

These considerations may already suffice to dictate the choice; however it must also be borne in mind that the subsequent expansion of a preliminary system is often envisaged and the addition of hardware may not be possible without a complete redesign of the system which it is desired to improve. With a microprocessor, the extension may be rapidly carried out by minor software modifications.

5.3. *The problem of timing*

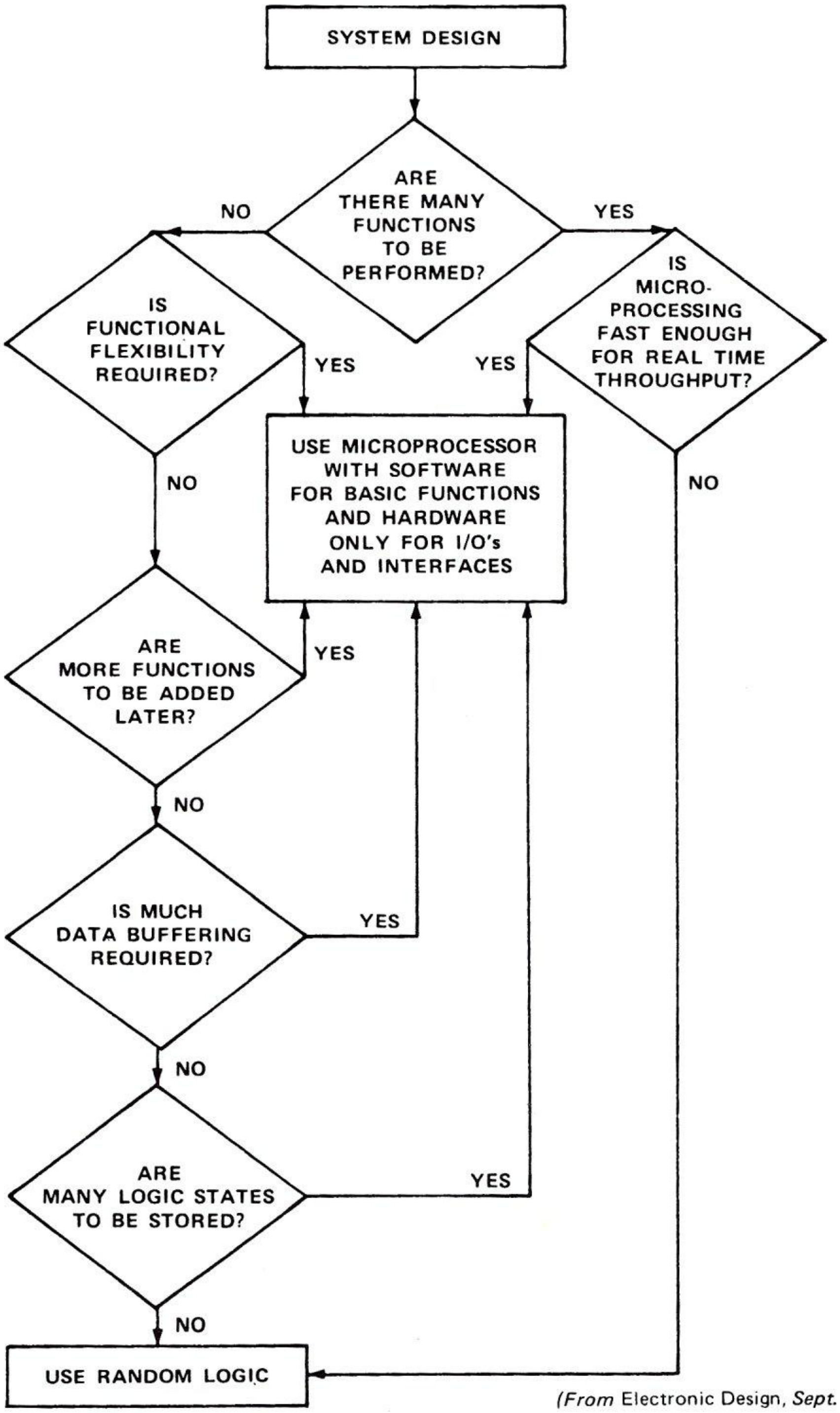
Have the functions of the system to be performed rapidly or not?

5.4. *Memory requirements*

How much data is to be processed?

Is a lengthy programme necessary for processing the data?

The above questions and the answers to them which govern the final decision may be schematically represented by means of the flowchart given on the next page.


SYSTEM DESIGN
ARE THERE MANY FUNCTIONS TO BE PERFORMED?
NO
YES
IS FUNCTIONAL FLEXIBILITY REQUIRED?
YES
NO
IS MICRO-PROCESSING FAST ENOUGH FOR REAL TIME THROUGHPUT?
YES
NO
USE MICROPROCESSOR WITH SOFTWARE FOR BASIC FUNCTIONS AND HARDWARE ONLY FOR I/O's AND INTERFACES
ARE MORE FUNCTIONS TO BE ADDED LATER?
YES
NO
IS MUCH DATA BUFFERING REQUIRED?
YES
NO
ARE MANY LOGIC STATES TO BE STORED?
YES
NO
USE RANDOM LOGIC

(From Electronic Design, *Sept. 1, 1973.)*

Random logic or microcomputer? That's a question system designers will be asking themselves more and more, when microprocessors become commonplace and inexpensive. The above flow chart lists basic considerations leading to a first-order decision.

Chapter II

THE MOTOROLA M6800 SYSTEM –PRESENTATION

In this chapter we shall attempt to identify in the M6800 family the general characteristics of a computer as previously described. We shall do this, not by dwelling uniquely on the MC6800 microprocessor but in demonstrating the extreme importance of the "blocks" which may be built on to the MPU (the central unit of the system) and which contribute the essential functions of every computer, namely, the memory and interface functions. On the other hand, we will not attempt to give a detailed description of each block considered separately, as this is done in the hardware manual. Instead, we will endeavour to show the interaction of the different blocks in the overall system because, in our opinion, it is the possibility of having available a total computer system which makes the M6800 family so powerful.

1. The M6800 family: a computer system

The M6800 family groups together the different components necessary for a computer-type architecture and functioning. Figure 1 shows the minimum computer system which it is possible to construct; in the figure may be found:

- an MC6800 microprocessor which is the heart of the system; this is the central unit which ensures the calculation and control functions;
- a memory which consists of a block of random access memory (RAM MCM6810) combined with a block of read only memory (ROM MCM6830);
- an I/O interface system consisting of a Peripheral Interface Adapter PIA MC6820 which allows access to the two peripherals.

In order to arrive at a minimum system it thus suffices to correctly interconnect the different blocks, to supply each of them with a single voltage of + 5 V and to connect a 2 phase clock to the MPU. In addition, a POWERFAIL/RESTART system must also enable the initial state of the system to be set.

When the need to "correctly interconnect the block" is specified, this means that all the pins reserved for data must be connected between themselves to constitute the data bus and above all to connect certain pins of the Bus Address to certain pins of the ROM or RAM and of the PIA, these connections allowing the MPU to address these different components. In this way, an address or a range of addresses is assigned to the memories and to the peripheral at the same time.

Thus, Figure 1 shows that the MPU will be able to address:

- the ROM when $A_{13} = A_{14} = 1$, the particular address in the ROM being selected by $A_0 - A_9$;
- the RAM when $A_{13} = A_{14} = 0$, the particular address in the RAM being selected by $A_0 - A_6$;
- the PIA when $A_{13} = 1$, $A_{14} = 0$, $A_3 = 1$ while the lines A_0 and A_1 will allow the selection of one of the four internal registers of the PIA which we will discuss later.

This configuration calls for the following comments:

- it is possible to choose for oneself the range of addresses covered by each block of memory, the essential point being that they do not overlap each other;
- the Data Bus comprising 8 lines and the address in the RAM being selected by 7 bits, it can be deduced that the capacity of the MCM6810 RAM is 128 bytes;
- similarly, the capacity of the MCM6830 ROM is 1024 = 1 K byte (address selected by 10 bits);
- a PIA has an address; there is therefore no distinction to be made between a peripheral addressable by the PIA and memory; in particular, the exchange of data with the outside is not governed by a set of instructions appropriate to each peripheral but by the same set of instructions which is used for handling the information in the memory;
- the presence of an IRQ pin (Interrupt Request Line) on the MPU should be noted. The MPU thus has the ability to transfer data by interruption (see part one, chapter IV, 2.4.);
- the minimum system can be expanded relatively simply, the only concern of the designer being to ensure that there is no intersection of the addresses covered by the different blocks. An example of expansion is given in Figure 2.;
- the Address Bus being composed of 16 lines, it may be deduced that it is possible to address 2^{16} = 64 K bytes. (Positions occupied by either memories or interface systems; see Figure (3)).

2. The Processor

Compared with the internal organization of the central unit of a computer given in Part I, the MPU MC6800 processor has several special characteristics although evidently comprising the various sub-systems necessary for its operation. The main peculiarities visible in Figure 4 are:

- the existence of two Accumulator registers A and B with a capacity of 8 bits, each of the accumulators allowing arithmetic and logical operations to be carried out;
- the status register is composed of 6 flip-flops, the 5 usual ones (Interrupt Mask, negative, zero, overflow, carry or link) plus a flip-flop H designated *"Half carry"* facilitating decimal calculations. The representation of the status register, also known as the "Condition Codes Register", is as follows:

7							0
		H	I	N	Z	V	C

Condition Codes Register

- the existence of a 16 bit register termed *"Stack Pointer Register"* which allows Stacking operations to be effected and which will be discussed below;
- the existence of a 16 bit register termed *"Index Register"* which is particularly useful for addressing tabulated data (see indexed addressing, 3.4.).

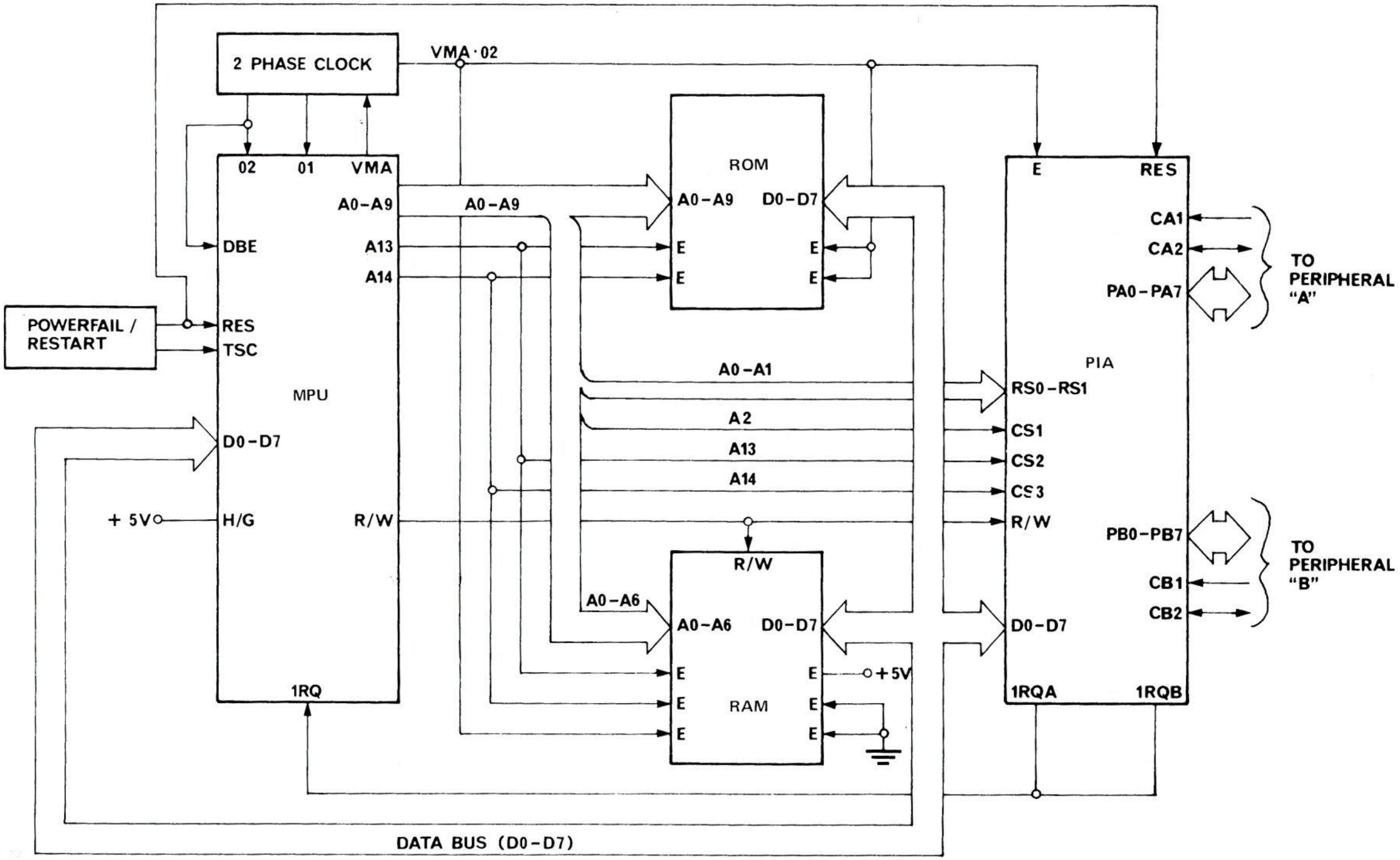

2 PHASE CLOCK
VMA · 02
02
01
VMA
MPU
A0–A9
A13
A14
DBE
POWERFAIL / RESTART
RES
TSC
D0–D7
+ 5V
H/G
R/W
1RQ
ROM
A0–A9
D0–D7
E
E
E
E
A0–A9
A0–A1
A2
A13
A14
A0–A6
RAM
R/W
A0–A6
D0–D7
E
E
E
E
E
E
+5V
PIA
E
RES
CA1
CA2
PA0–PA7
TO PERIPHERAL "A"
RS0–RS1
CS1
CS2
CS3
R/W
PB0–PB7
TO PERIPHERAL "B"
CB1
CB2
D0–D7
1RQA
1RQB
DATA BUS (D0–D7)

FIGURE (1). MINIMUM COMPUTER SYSTEM

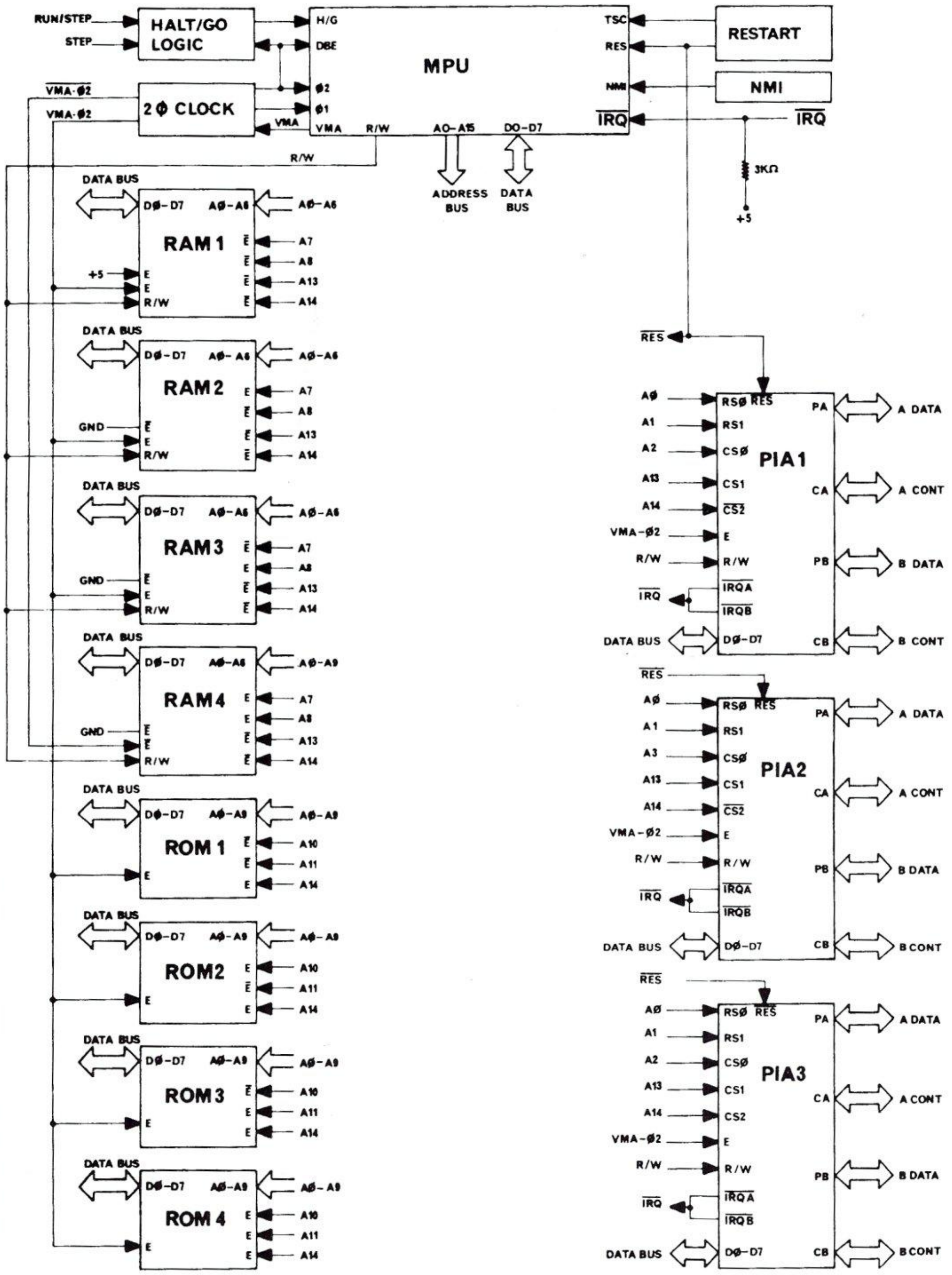

RUN/STEP
STEP
HALT/GO LOGIC
MPU
H/G
DBE
φ2
φ1
VMA
R/W
A0–A15
D0–D7
TSC
RES
NMI
IRQ
RESTART
NMI
IRQ
VMA·φ2
VMA·φ2
2 φ CLOCK
VMA
R/W
ADDRESS BUS
DATA BUS
3KΩ
+5
DATA BUS
D0–D7
A0–A6
RAM 1
Ē
A7
A8
A13
A14
+5
E
R/W
RAM 2
GND
RAM 3
RAM 4
A0–A9
ROM 1
ROM 2
ROM 3
ROM 4
A10
A11
RES
PIA1
PIA2
PIA3
RS0
RS1
CS0
CS1
CS2
A0
A1
A2
A3
VMA–φ2
R/W
IRQA
IRQB
PA
CA
PB
CB
A DATA
A CONT
B DATA
B CONT

FIGURE (2) SYSTEM EXPANSION

Address

Device	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAM 1	d	0	0	d	d	d	d	0	0	X	X	X	X	X	X	X
RAM 2	d	0	0	d	d	d	d	0	1	X	X	X	X	X	X	X
RAM 3	d	0	0	d	d	d	d	1	0	X	X	X	X	X	X	X
RAM 4	d	0	0	d	d	d	d	1	1	X	X	X	X	X	X	X
ROM 1	d	1	0	d	0	0	X	X	X	X	X	X	X	X	X	X
ROM 2	d	1	0	d	0	1	X	X	X	X	X	X	X	X	X	X
ROM 3	d	1	0	d	1	0	X	X	X	X	X	X	X	X	X	X
ROM 4	d	1	0	d	1	1	X	X	X	X	X	X	X	X	X	X
PIA 1	d	0	1	d	d	d	d	d	d	d	d	0	0	1	X	X
PIA 2	d	0	1	d	d	d	d	d	d	d	d	0	1	0	X	X
PIA 3	d	0	1	d	d	d	d	d	d	d	d	1	0	0	X	X

d = dont' care X = variable address 0 = Logical zero 1 = Logical one

FIGURE (3) DEVICE SELECT ADDRESSING

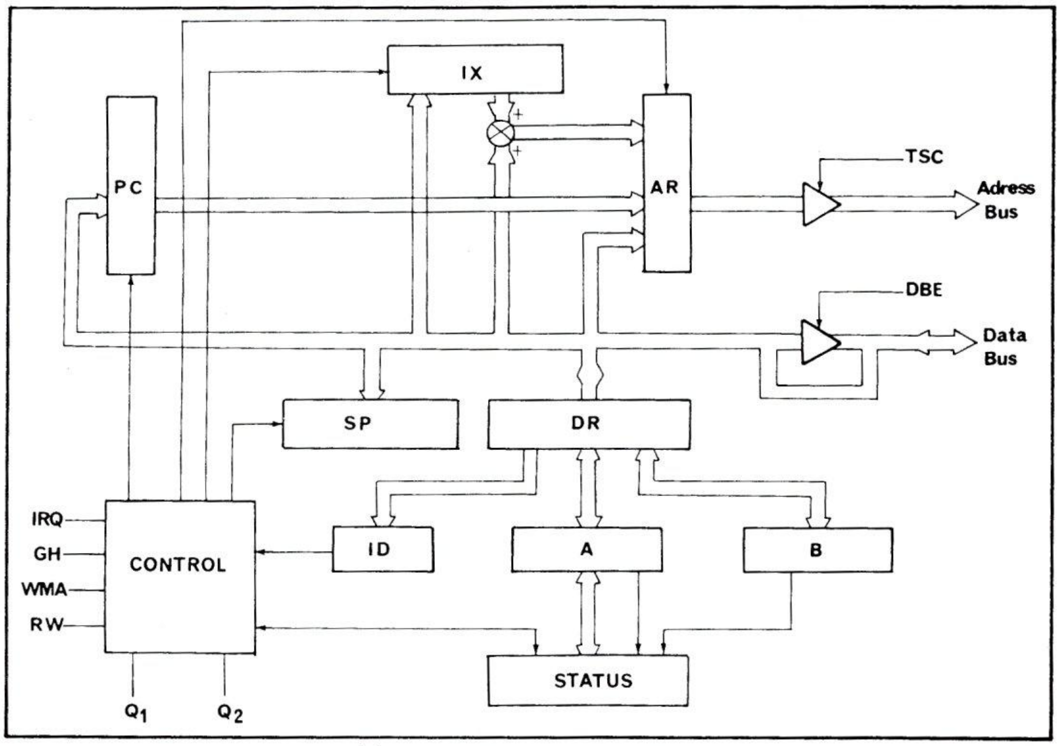

IX
+
+
PC
AR
TSC
Adress Bus
DBE
Data Bus
SP
DR
IRQ
GH
WMA
RW
CONTROL
ID
A
B
STATUS
Q1
Q2

FIGURE (4) MC6800 MPU INTERNAL CONFIGURATION

3. The utility of the additional units of the CPU

3.1. *The two accumulators ACCA and ACCB*

The fact that two accumulators are available allows in particular the storage of a partial result in ACCB for example while a calculation is accomplished in ACCA. The utility of this is obvious when it is known that it is faster to store a partial result in an accumulator than in the memory where it would subsequently have to be fetched; in addition, it is possible to do a calculation in the second accumulator ACCB. The two accumulators allow a saving in:

- time to execute;
- memory positions (fewer instructions).

This comes out clearly in the following example in which the value 5x/2 is to be calculated for each value of x read from a peripheral:

Computer with two Accumulators

	Machine Cycles
Read input x in ACCA	
Transfer ACCA ⟶ ACCB	2
Calculate x/2 in ACCA	2
Calculate 2x in ACCB	2
Result: ACCA + ACCB ⟶ ACCA	2
	8

Computer with one Accumulator only

Machine Cycles	
	Read input x in ACCA
4	Transfer ACCA to MEM1
2	Calculate x/2 in ACCA
4	Store ACCA in MEM2
3	Load ACCA with MEM1
2	Calculate 2x in ACCA
3	Result: ACCA + MEM2 ⟶ ACCA
18	

Opposite each instruction is written the time of execution in μs; we note that the total time of execution is 8 μs for a computer with two accumulators (MC6800) while it would be 18 μs if the same MPU had only a single accumulator. The difference in the number of instructions should also be noted.

3.2. *Function of the "Half-carry" flip-flop H*

In order to elucidate the function of this flip-flop it is useful to have another look at BCD notation and arithmetic. Suppose the decimal addition 13 + 28 has to be accomplished. The MPU MC6800 allows this to be done without the need to convert the two operands into pure binary and then reconvert the binary result into a BCD number.

In a first phase the MPU carries out the binary addition as follows:

$$\begin{array}{rl} 13 & 0001\ 0011 \\ +\ 28 & 0010\ 1000 \\ \hline & 0011\ 1011 \end{array}$$

We note that the least significant group is not meaningful in the BCD code, this binary number 1011 being greater than 1001. It is necessary to make a correction equal to + 6 to obtain the right result:

$$\begin{array}{rl} & 0011\ 1011 \\ +6 & 0000\ 0110 \\ \hline & 0100\ 0001 \end{array}$$

The correction, made by means of a special instruction DAA (Decimal Adjust, A), gives rise to a carry on the bit 4 of the least significant group; the existence of this carry digit affects the flip-flop H which in this case will be set to 1. In a second phase the DAA instruction will perform the addition of this carried digit to the most significant BCD group to give the correct result 0100 0001 = 41.

$$\begin{array}{rll} & 0011\ 1011 & \\ + & 0000\ 0110 & \\ \hline & 0011\ 0001 & \\ + & 0001 & \longleftarrow \text{Carry From Bit 4} \\ \hline & 0100\ 0001 & \end{array}$$

Note: The positioning of the flip-flop H does not depend on the particular arithmetic used. The flip-flop H is also active during a binary addition which gives rise to a carry on the bit 4.

3.3. *Stack Pointer*

The stack pointer is of great importance in processing interruptions and subroutines.

3.3.1. *Definition of the stack*

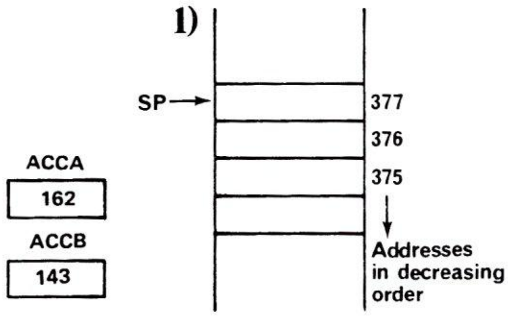
A Stack designates a portion of the memory used for the temporary storage of one or several items of information.

A stack is sometimes described as a LIFO device (Last In, First Out); this designation is justified by the operation of the stack which is explained below:

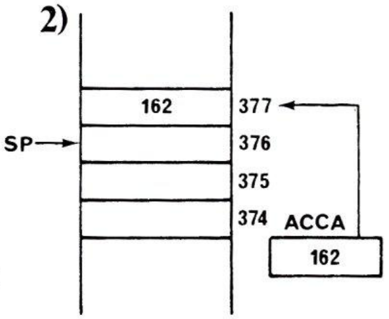
The processing of a stack involves two operations:

- an operation termed "pushing" which allows the stack to be filled from an accumulator;
- an operation termed "pulling" which allows the stack to be emptied, i.e., to have elements removed from it and transferred to the accumulator.

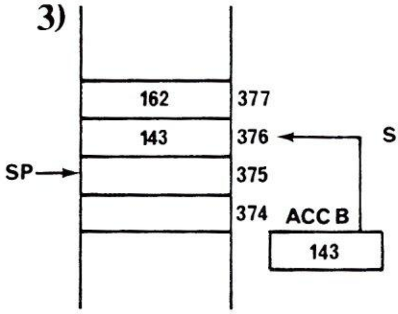
The pushing or the pulling take place in the memory position indicated by the stack pointer SP. The two operations may be schematically represented as follows:



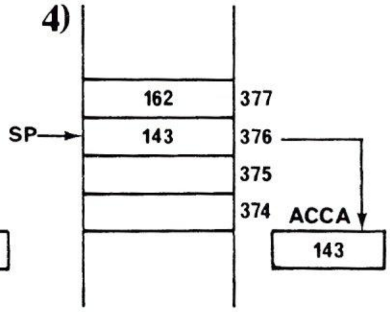
Initial State



Push ACCA



Push ACCB



Pull ACCA

Note:

- in every programme using the stack, the stack pointer must be reset to its initial value;
- the stack pointer being a 16 bit register addressing 64 K bytes, it is possible to construct a stack in any part of the memory (except of course in the addresses reserved for the programme)
- on pushing, there is a transfer of the contents of the accumulator to the address indicated by the stack pointer and *then decrementation* of the latter by one;
- on pulling, there is *incrementation* of the stack pointer and *then* transfer of the contents of the memory position indicated by the stack pointer to the accumulator.

3.3.2. *Other uses*

We have just seen that it is possible to make transfers from one of the accumulators to the stack or vice versa with the aid of the *programmed* operations of pushing and pulling; however, this is only a particular case of usage of the stack.

The most common utilization is during operations of interruption or jumping to a subroutine in which pushing and pulling are *automatically* accomplished. This will be treated in the next chapter.

3.4. *Index register – Indexed addressing*

This 16 bit register facilitates access to the sequential data stored in the memory. The address of the item of data it is desired to reach can be obtained by adding the contents of the index register X to a constant base C:

address = C + X

Clearly, it is easy to obtain access to sequential data by causing X to change by one unit.

4. One of the interface systems: the PIA

One of the principal advantages of the M6800 family is certainly the provision of this circuit with so many possibilities; the PIA clearly demonstrates the philosophy of the microprocessor, with which any evolution of a given system can be achieved with software and possibly minor hardware changes.

Physically, the PIA (Peripheral Interface Adapter) is a package the size of the MPU (40 pins) which allows access by means of two two-way buses to most of the peripherals necessitating 8 bits of Data. Figures at pages 41 and 42 show the internal organization of the PIA; it can be seen that the PIA comprises two parts A and B which are almost identical and of which the outputs consists of two groups of 8 lines PA_0–PA_7 and PB_0–PB_7 respectively; these are the Data lines of communication of the PIA with the peripheral(s). On the other hand, PIA–MPU communication is provided by only 8 lines of data, D_0–D_7, the MPU working on bytes.

The other MPU–PIA links are:

- the 3 Chip Select lines CS_0, CS_1, $\overline{CS_2}$ connected to the Bus Address and which allow overall addressing of the PIA;
- the two Register Select lines RS_0, RS_1 which allow addressing of the internal registers of the PIA;
- the R/$\overline{W}$ line which permits the MPU to read to PIA (R/W = 1) or alternatively to write information there (R/$\overline{W}$ = 0);
- the Enable line which permits synchronization in reading or writing;
- the Reset line which sets the internal registers of the PIA to their initial values when the system is connected to the power supply;
- the 2 interrupt request lines IRQA and IRQB which enable the PIA to interrupt the MPU when necessary. The MPU has only one IRQ pin (Interrupt request) and the two lines IRQA and IRQB must be either OR-wired to the IRQ alternatively arrive there via an interrupt priority circuit when the polling of devices having requested the interruption is not desirable by means of Software.

As regards the PIA-peripheral(s) lines, these comprise:

- 16 Data lines PA_0 – PA_7 and PB_0 – PB_7, each of these lines being programmable as either input or output;
- 4 lines CA_1, CA_2 and CB_1, CB_2 of which the action on the PIA or the peripheral is programmable.

  CA_1 and CB_1 are uniquely input lines to the PIA and in certain conditions act on the interrupt request lines IRQA and IRQB.

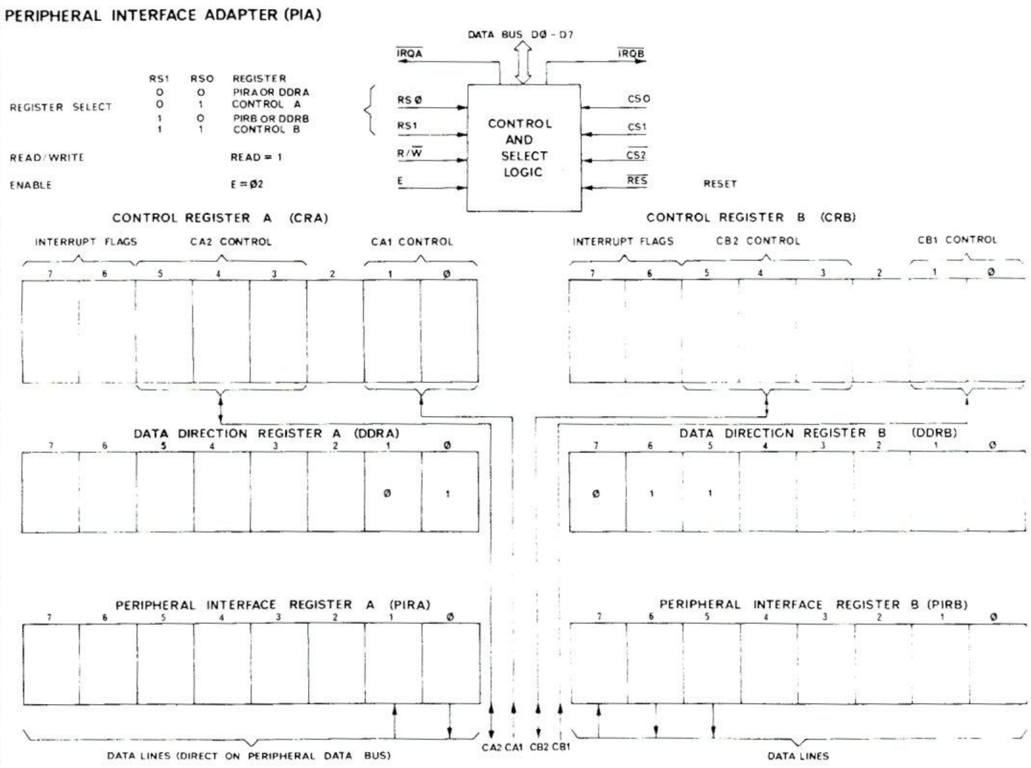
  CA_2 and CB_2 which have the same possibility as CA_1 and CB_1 may in addition be used as peripheral control outputs (possibility of generating levels or strobes).

Each of the two parts A and B of the PIA incorporates the two registers necessary for interfacing a CPU with a peripheral, viz.,

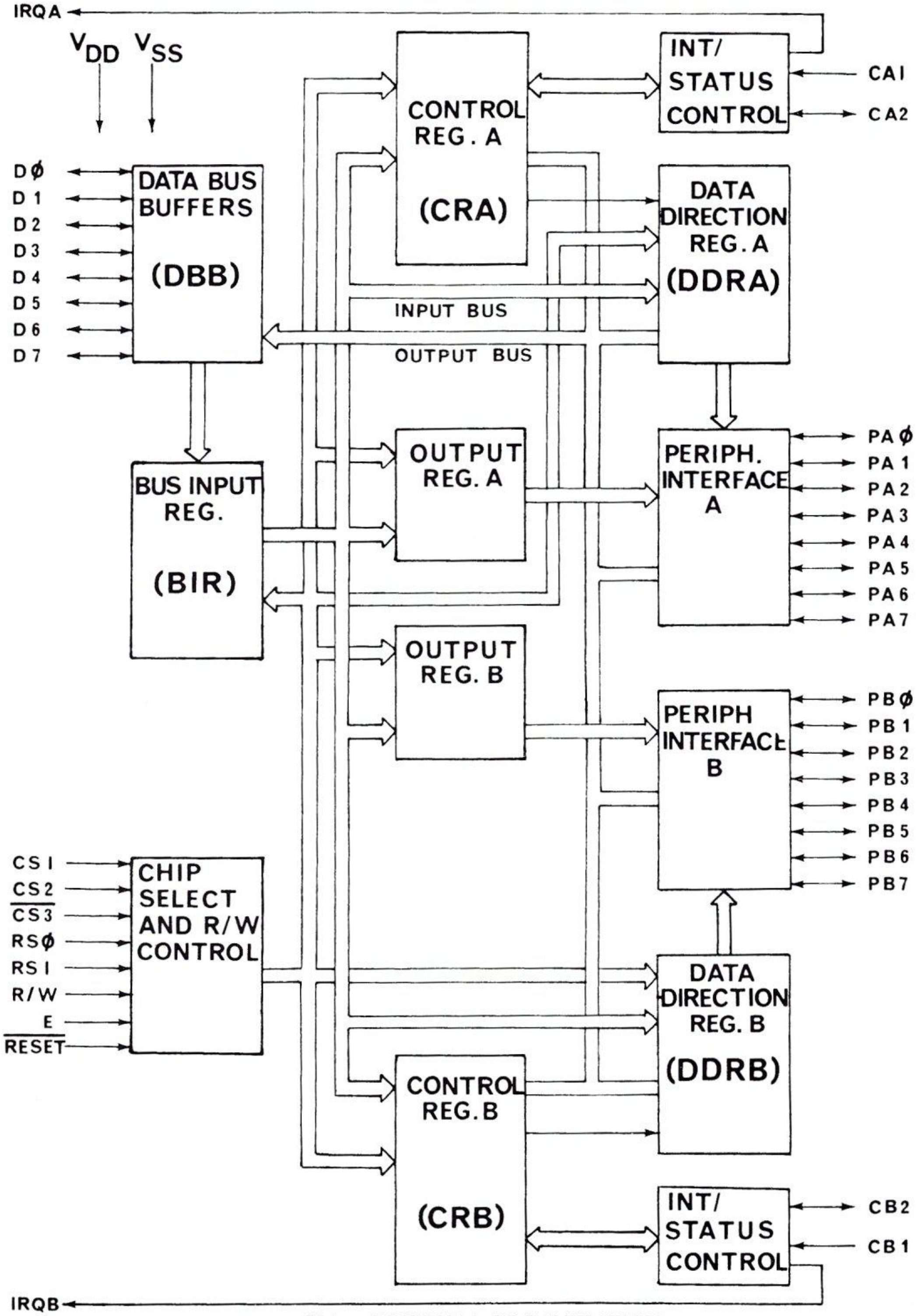
- a Data register (PIR A or PIR B);
- a control register (CRA or CRB).

Also to be noted is the existence of a register termed the "Data Direction Register" which allows each Data line to be programmed as an input or an output.

This concludes the brief presentation of the function and configuration of the PIA; in order to make most use of the power of this unit, the effect of the 4 lines CA_1, CA_2, CB_1, CB_2 on either the PIA or the peripheral must be examined in detail; this is done in the Hardware Manual.


PERIPHERAL INTERFACE ADAPTER (PIA)
RS1 RSO REGISTER
0 0 PIRA OR DDRA
0 1 CONTROL A
1 0 PIRB OR DDRB
1 1 CONTROL B
REGISTER SELECT
READ/WRITE
READ = 1
ENABLE
E = 02
DATA BUS D0 - D7
$\overline{IRQA}$
$\overline{IRQB}$
RS0
RS1
R/$\overline{W}$
E
CONTROL AND SELECT LOGIC
CS0
CS1
$\overline{CS2}$
$\overline{RES}$
RESET
CONTROL REGISTER A (CRA)
INTERRUPT FLAGS
CA2 CONTROL
CA1 CONTROL
7 6 5 4 3 2 1 0
CONTROL REGISTER B (CRB)
INTERRUPT FLAGS
CB2 CONTROL
CB1 CONTROL
7 6 5 4 3 2 1 0
DATA DIRECTION REGISTER A (DDRA)
7 6 5 4 3 2 1 0
0
1
DATA DIRECTION REGISTER B (DDRB)
7 6 5 4 3 2 1 0
0
1
1
PERIPHERAL INTERFACE REGISTER A (PIRA)
7 6 5 4 3 2 1 0
PERIPHERAL INTERFACE REGISTER B (PIRB)
7 6 5 4 3 2 1 0
DATA LINES (DIRECT ON PERIPHERAL DATA BUS)
CA2 CA1 CB2 CB1
DATA LINES

PIA REGISTERS



IRQA
VDD
VSS
CONTROL REG. A
(CRA)
INT/ STATUS CONTROL
CA1
CA2
D0
D1
D2
D3
D4
D5
D6
D7
DATA BUS BUFFERS
(DBB)
DATA DIRECTION REG. A
(DDRA)
INPUT BUS
OUTPUT BUS
BUS INPUT REG.
(BIR)
OUTPUT REG. A
PERIPH. INTERFACE A
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
OUTPUT REG. B
PERIPH INTERFACE B
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
CS1
CS2
CS3
RS0
RS1
R/W
E
RESET
CHIP SELECT AND R/W CONTROL
DATA DIRECTION REG. B
(DDRB)
CONTROL REG. B
(CRB)
INT/ STATUS CONTROL
CB2
CB1
IRQB

PIA INTERNAL ORGANIZATION

(To Be Continued Next Month)

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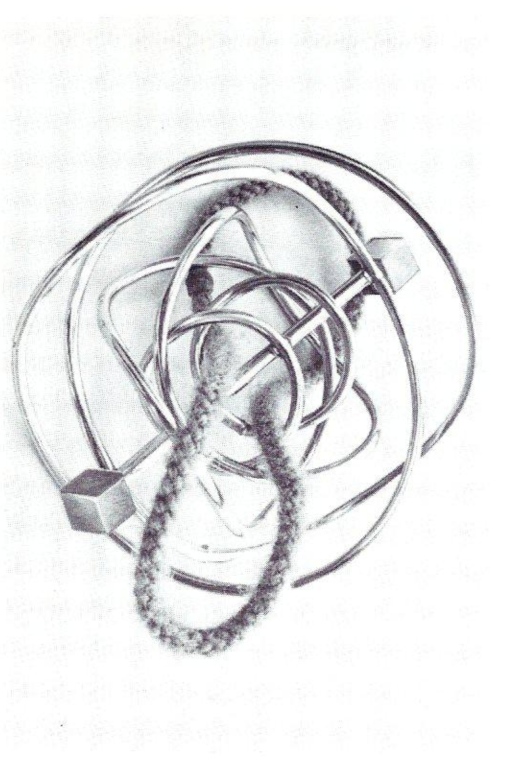

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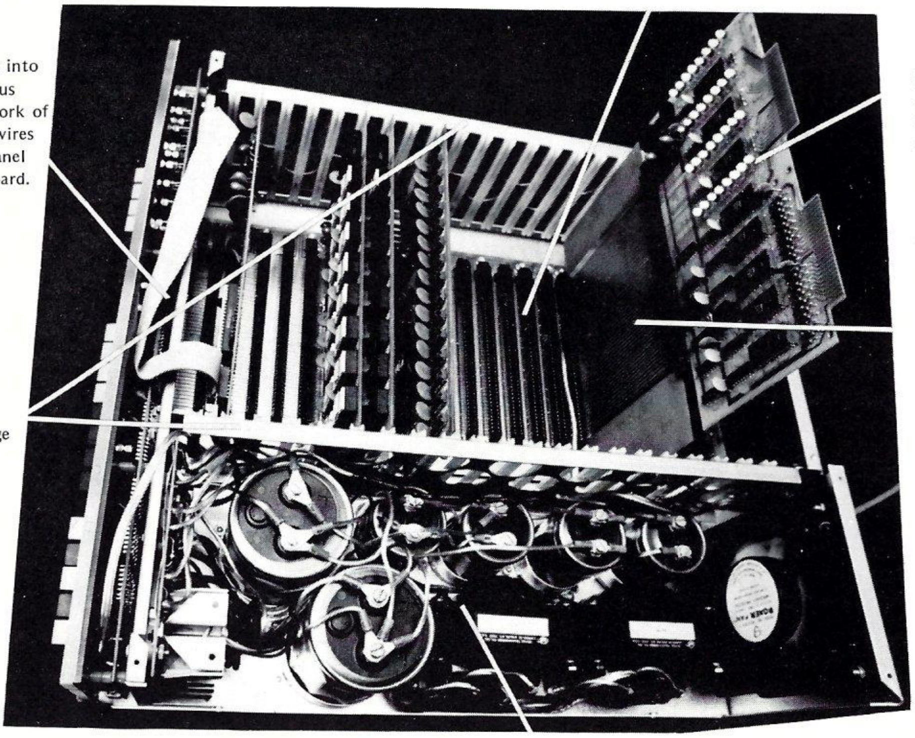

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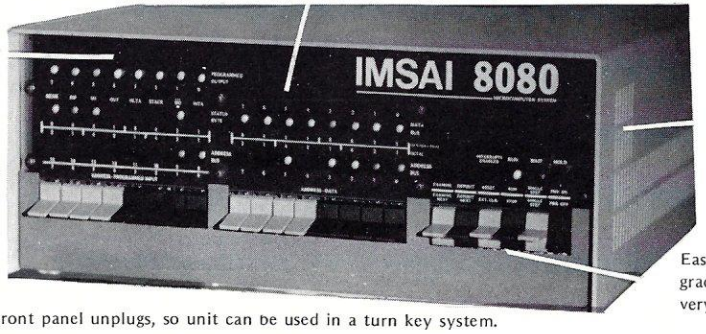

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